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MT8127 Design Notice

V0.2

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MT8127 Design Notice Version History

- **MT8127 Baseband Design Notice**

Category	Description	Date	Version	Remark
BB	BB Design Notice		V0.1	OK
BB	GPIO Application Notice		V0.1	OK
BB	BB Schematic Design Notice		V0.1	OK
BB	SD & eMMC Design Note		V0.1	OK
BB	Camera Design Notice		V0.1	OK
BB	USB Design Notice		V0.1	OK
BB	LCM Design Notice		V0.1	OK

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Change List

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Change List

Version	Date	Description
V0.1	2014.02.25	1st release
V0.2	2014.03.03	2nd release 1.Add DPI Panel Design notice 2.Update MT8127 Feature comparison page (P.5)

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MT8127 Feature comparison

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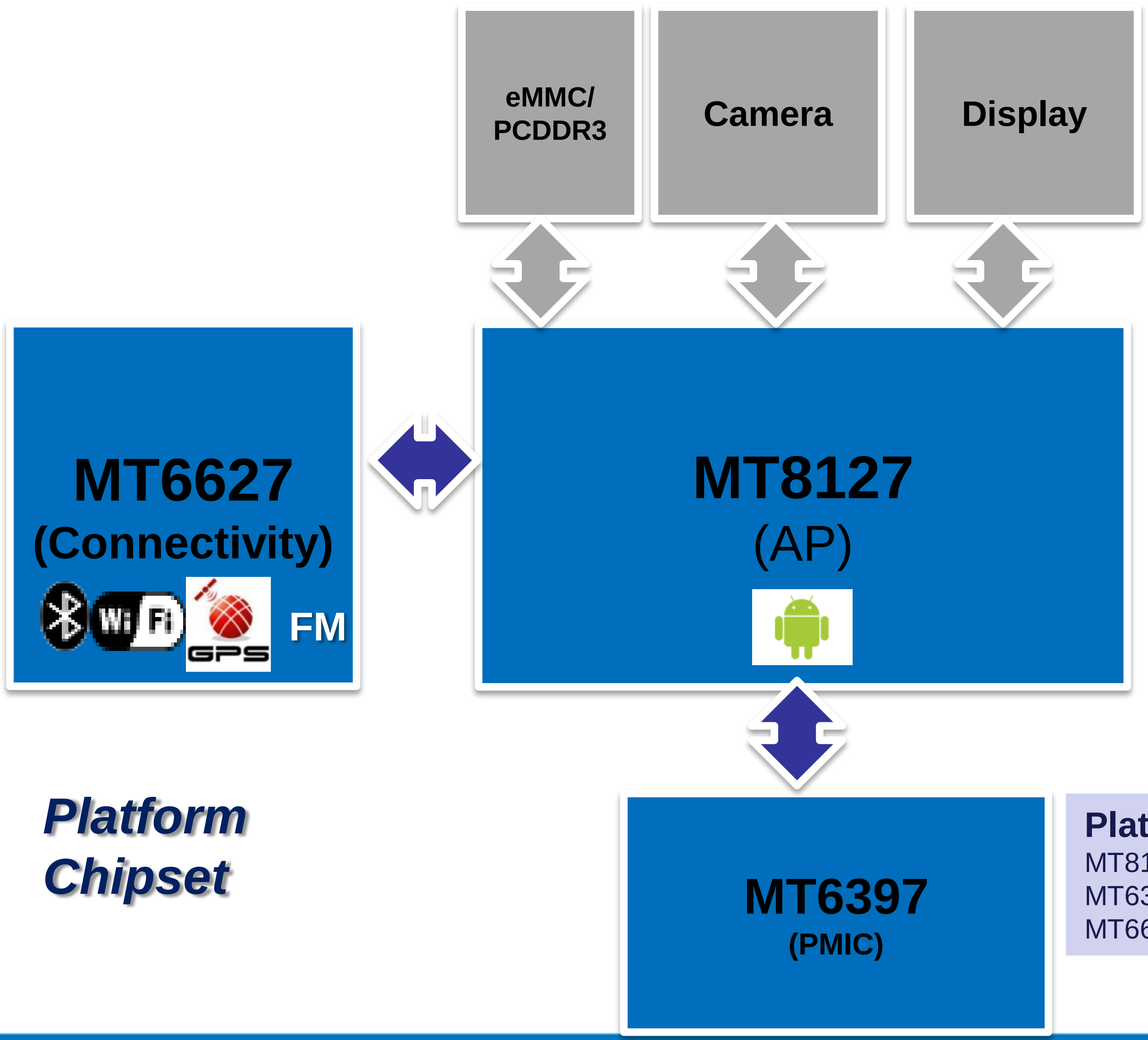
	MT8127T	MT8127	MT8117S	MT8117
Apps CPU	Cortex-A7 x 4, 1.5GHz	Cortex-A7 x 4, 1.3GHz	Cortex-A7 x 3, 1.3GHz	Cortex-A7 x 2, 1.3GHz
Graphics	Mali-450 MP4@500MHz 108Mtri/s, 2.0Gpix/s	Mali-450 MP4@416MHz 90Mtri/s, 1.6Gpix/s	Mali-450 MP3@416MHz 68Mtri/s, 1.2Gpix/s	Mali-450 MP3@416MHz 68Mtri/s, 1.2Gpix/s
Memory	DDR3x32 **1333Mbps**	DDR3x32 **1333Mbps**	DDR3x32 **1333Mbps**	DDR3x32 **1333Mbps**
Camera	**13MP ISP**	**13MP ISP**	**13MP ISP**	**13MP ISP**
Video Decode	1080p 30fps **HEVC** / MPEG-4 / H.264 / VC-1	1080p 30fps **HEVC** / MPEG-4 / H.264 / VC-1	1080p 30fps **HEVC** / MPEG-4 / H.264 / VC-1	1080p 30fps **HEVC** / MPEG-4 / H.264 / VC-1
Video Encode	1080p 30fps	1080p 30fps	1080p 30fps	1080p 30fps
Display	**WUXGA 1920x1200 MIPI / LVDS Built-in HDMI**	**WXGA 1280x800 MIPI / LVDS Built-in HDMI**	**WXGA 1280x800 MIPI / LVDS Built-in HDMI**	**WXGA 1280x800 MIPI / LVDS Built-in HDMI**
Connectivity	**Embedded Wi-Fi bgn/BT/FM/GPS BB**	**Embedded Wi-Fi bgn/BT/FM/GPS BB**	**Embedded Wi-Fi bgn/BT/FM/GPS BB**	**Embedded Wi-Fi bgn/BT/FM/GPS BB**
Speaker AMP	**Stereo Class-D (MT6397)/Mono Class-D (MT6323)**			
PMIC	**MT6323+2A Buck (No MHL Support) MT6397**		**MT6323 (No MHL Support) MT6397**	
PCB	**Normal PCB 4-layer**	**Normal PCB 4-layer**	**Normal PCB 4-layer**	**Normal PCB 4-layer**

MT8127 Platform Block Diagram



Platform Chipset

Platform Chipset:
MT8127: 12.1x12.6x1.2mm, 0.5P x393 TFBGA
MT6397: 11x11.7x1.1mm, 0.65P x211 TFBGA
MT6627: 5x5x0.9mm, 40 QFN

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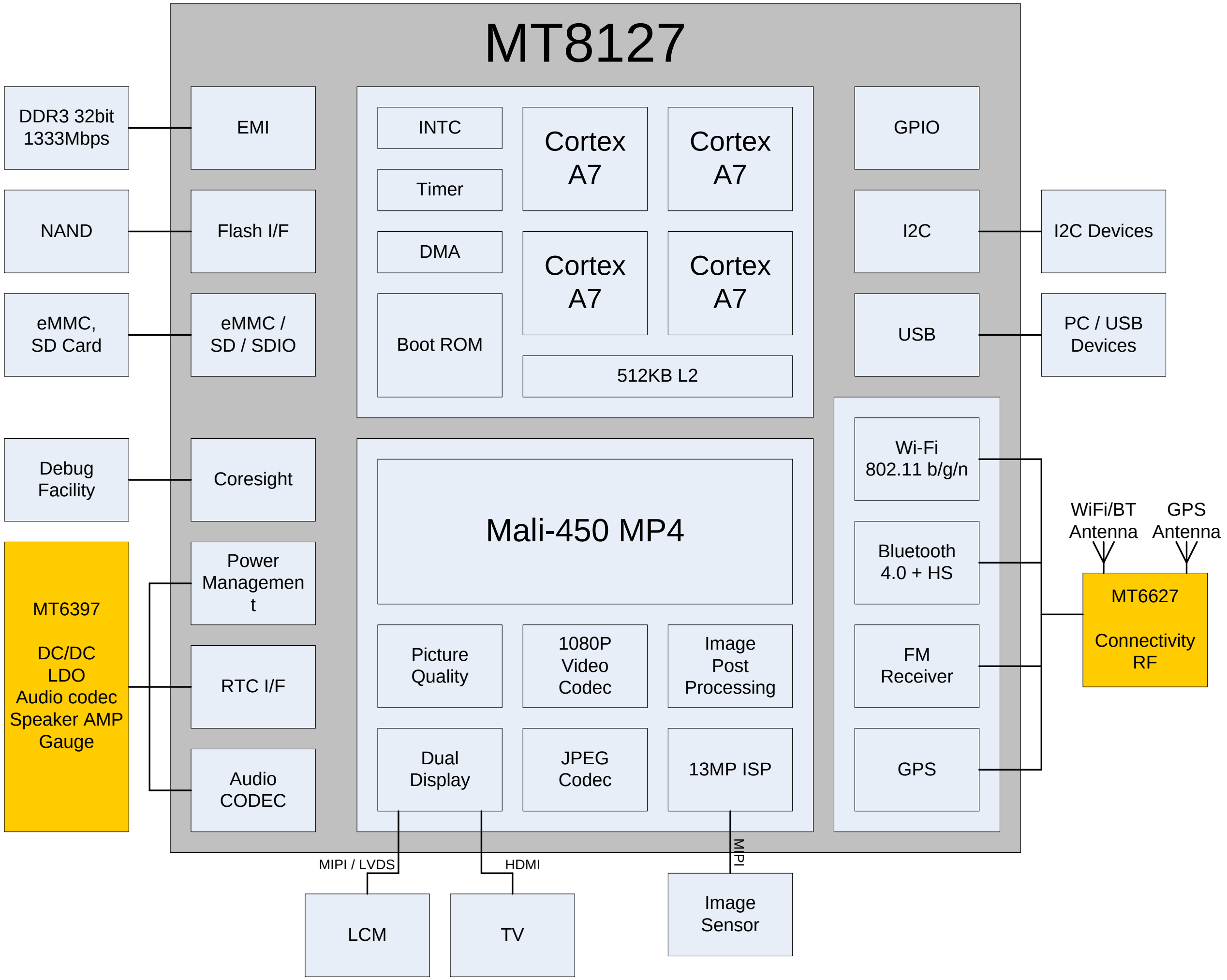
Block diagram of MT8127



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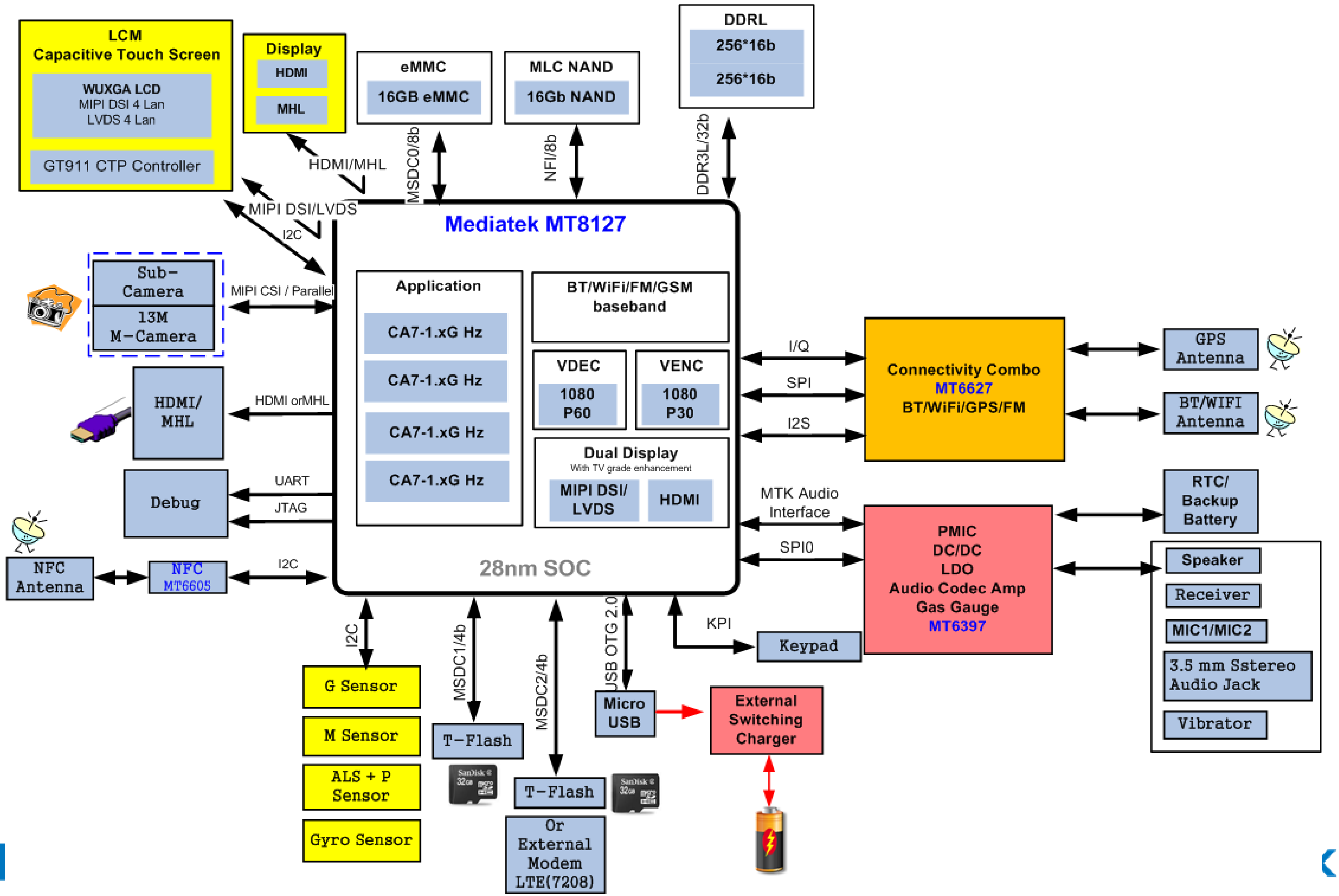
MT8127 System Block Introduction



Internal Use

MT8127 Ball Map

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MT8127 Ball Map – DDR3L x16

393	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
A	GNDK	ED1	ED5	ED4		ED13	ED11	ECKE		EA1		EA5	EA9	ECS0	ERAS	EBA2		ED30	ED17	ED21	ED20	ED18	ED31	GNDK	A
B	ED10	ED14	ED3	ED7	ED2	ED15	GNDK	EA10	EA8	EA4	EBA1	EA3	EA13	ERWE	ECAS	ECS1	ED24	ED26	ED28	ED19	ED22	ED16	ED25	ED27	B
C	REXT DN	ED8	ED12	ED6	ED0	ED9	EDQM 1		EA14	EA6	EA0	GNDK		GNDK	ERESE T	GNDK		EDQM 2		GNDK	ED23	ED29	MSDC 0_DAT	MSDC 0_DAT	C
D	MSDC 1_CLK	MSDC 1_DAT	MSDC 1_DAT			EDQS1	GNDK			GNDK	EA7			EBA0	ECL K1			EDQ S3	GNDK	EDQM 3		MSDC 0_DAT	MSDC 0_DAT	MSDC 0_DAT	D
E		MSDC 1_DAT	MSDC 1_CM	EDQM 0		EDQS1 _B		EDQS0		ECL K0_B	EA12			EA2	ECL K1_B			EDQ S3_B				MSDC 0_DAT	MSDC 0_DAT		E
F	DVDD 18_IO2	MSDC 1_DAT	CMM CLK	GNDK		GNDK		EDQS0 _B		ECL K0	EA11			EA15	AVSS1 8_ME			TP_ME MPLL	EDQ S2	EDQ S2_B	GNDK	MSDC 0_DAT	EINT14	MSDC 0_RST	F
G	DVDD 28_MS			CMDA T1	CMDA T0	CMPC LK	VCCIO	VCCIO		VREF2	VCCIO			VCCIO	VREF1		VCCIO	VCCIO	AVDD 18_ME	MSDC 0_CM	MSDC 0_CLK	GNDK	EINT15	DVDD 28_MS	G
H		RDN0_ A	RDP0_ A					VCCIO		VCCIO		GNDK	GNDK		VCCIO								EINT16		H
J	DVDD 18_MI	RDN1_ A	RDP1_ A	RCP_A	RCN_ A	DVSS1 8_MIPI					VCCK			VCCK								EINT17	EINT21	DVDD 28_NFI	J
K	RDN0	RDP0					DVDD 18_EF	FSOU RCE_P	VCCK	GNDK	GNDK	GNDK		GNDK	VCCK		UTXD0	URXD 0	SDA2	SCL2	I2S_D ATA_I	AUD_ DAT_	AUD_ CLK_	AUD_ DAT_	K
L		RDN1	RDP1						VCCK	GNDK		GNDK	GNDK		VCCK		URXD 1	UTXD1	PWRA P_SPI0	I2S_B CK	I2S_LR CK	GNDK	PWRA P_INT		L
M	DVDD 18_MI	RDN2	RDP2	RCN	RCP	GNDK		VCCK		GNDK	GNDK	GNDK	GNDK	GNDK	GNDK							PWRA P_SPI0	PWRA P_SPI0	DVDD 18_IO0	M
N		RDN3	RDP3	DVSS1 8_MIPI		GNDK		VCCK		GNDK		GNDK	GNDK		GNDK							PWRA P_SPI0	PWRA P_SPI0		N
P	VRT	TDP0	TDN0					VCCK		GNDK	GNDK	GNDK	GNDK	GNDK	GNDK	AVSS3 3_VDA		VCCK _VPRO	VCCK _VPRO		AVDD 33_VD	PWRA P_SPI0	SRCL KENAI	WATC HDOG	P
R		TDP1	TDN1	TCP	TCN	DVSS1 8_MIPI		VCCK	VCCK	GNDK		GNDK	GNDK		VCCK _VPRO		VCCK _VPRO	UTXD3	VCCK _VPRO	SYSRS TB	RTC32 K_CK	SRCL KENA	VDAC _C		R
T	TDP2	TDN2						MSDC 2_CLK		GNDK	GNDK	GNDK		VCCK _VPRO	VCCK _VPRO	VCCK _VPRO								DVDD 18_IO1	T
U	TDP3	TDN3	DVSS1 8_MIPI	DVDD 18_IO3	MSDC 2_DAT	MSDC 2_DAT	MSDC 2_CM			VCCK	VCCK	VCCK		VCCK _VPRO				URXD 3	URXD 2	UTXD2	PCM_ TX	PCM_ CLK	PCM_ SYNC	DVDD 28_DPI	U
V			MSDC 2_DAT	MSDC 2_DAT										VCCK _VPRO	VCCK _VPRO			JTMS		EINT20	EINT4	PCM_ RX	EINT12		V
W		DVDD 28_MS	SDA0	SCL0	LCM_ RST	DSI_T E	GNDK	GNDK		F2W_C LK	GNDK			AVSS1 8_PLL	GNDK			JTDI				EINT11	EINT9	EINT10	W
Y	WB_C RTL2	WB_C RTL3	WB_C RTL4	WB_C RTL5		AVSS1 8_WB	WB_S EN			F2W_D ATA	CHD_ DM_P0			AUX_I N0	AUX_I N1			JTDO	EINT3		EINT13		EINT7	EINT8	Y
AA	WB_C RTL0	WB_C RTL1			AVDD 18_WB	XIN_W BG	WB_S DATA			AVSS3 3_USB	CHD_ DP_P0			AUX_I N3	AUX_I N2			JTCK	EINT2		EINT1	GNDK	EINT6		AA
AB	WB_R XIP	WB_R XIN	AVSS1 8_WB				WB_S CLK		AVSS3 3_USB		AVDD 33_US			AVDD 18_HD	AUX_I N4			REFP	EINT0			EINT5	KPCO L0	KPRO W0	AB
AC	WB_R XQP	AVSS1 8_WB		AVSS1 8_WB		AVSS1 8_WB			USB_ VRT	AVDD 18_US		AVSS1 8_HD		AVDD 18_AP		AUX_I N5	AVSS1 8_AP	SPI_ CK	SPI_M I	DISP_ PWM	EINT19	KPCO L1	KPCO L2	KPRO W1	AC
AD	WB_R XQN	WB_T XIP	WB_T XQP	AVSS1 8_WB	GPS_R XIP	GPS_R XQP	WB_R STB	USB_D M_P1	USB_V BUS	USB_D M_P0		HDMI TX_CL	HDMI TX_CH	HDMI TX_CH	HDMI TX_CH		26M_ CLK	SPI_M O	SPI_C S	EINT18	HTPLG	HDMI SD	SCL1	KPRO W2	AD
AE	AVSS1 8_WB	WB_T XIN	WB_T XQN	AVSS1 8_WB	GPS_R XIN	GPS_R XQN	AVSS1 8_WB	USB_D P_P1		USB_D P_P0		HDMI TX_CL	HDMI TX_CH	HDMI TX_CH	HDMI TX_CH	HDMI TX_RE	TEST MODE		AVD D18_	GNDK	CEC	HDMI SCK	SDA1	GNDK	AE
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	

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GPIO Application Notice

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Design Notice – GPIO selection (1/x)

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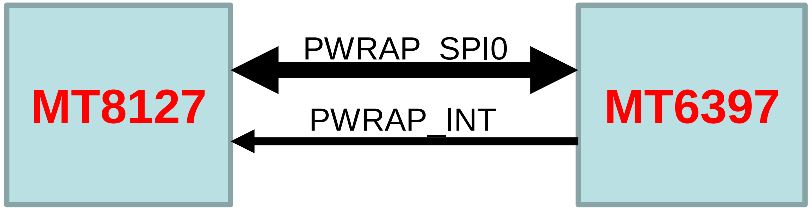
- *GPIO with 2.8v/3.3v power domain for 28nm should be careful*
- MT8127 GPIO
  - Supports x143 GPIOs belong to 11 Power Domains
  - Power Domain :
    - DVDD18_IO0 (1.8v)
    - DVDD18_IO1 (1.8v)
    - DVDD18_IO2 (1.8v)
    - DVDD18_IO3 (1.8v)
    - DVDD18_MIPIRX (1.8v)
    - DVDD18_MIPITX (1.8v)
    - DVDD28_DPI (1.8v/2.8v/3.3v)
    - DVDD28_NFI (1.8v/2.8v/3.3v)
    - DVDD28_MSDC0 (1.8v/2.8v/3.3v)
    - DVDD28_MSDC1 (1.8v/2.8v/3.3v)
    - DVDD28_MSDC2 (1.8v/2.8v/3.3v)

	MT8127	MT6397
GPIO Number	X143	x41
GPIO Mapping	GPIO 0~142	GPIO 0~40
EINT Number	x141	Not support
EINT Mapping	EINT 0~11 EINT14~142	Not support



- MT6397 (PMIC) GPIO extender
  - GPIO communicate to MT8135 through SPI interface
  - GPIO extender with x41 GPIOs which only supports 1.8v IO level.
- IF no GPIO are used for specific power domain, please set to 1.8v

☆GPIO Mapping & EINT Mapping Please refer to MT8127 GPIO Table☆

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Design Notice – GPIO selection (2/x)

- **Pull-Up / Pull-Down selection :**
  - Choose GPIO with suitable PU/PD after reset state for application
    - Ex : As for “enable pin of audio amplifier”, please choose GPIO with **PD** after reset state
    - Ex : As for “enable pin of external LDO”, please choose GPIO with **PD** after reset state
- **Power domain of IO supply selection :**
  - Choose GPIO with suitable power domain of IO supply for application
- **Please choose suitable GPIO for peripheral IC :**
  - Please choose GPIOs with matched direction, pull-up/pull-down, data inversion, data output, gpio mode after reset state for peripheral IC application

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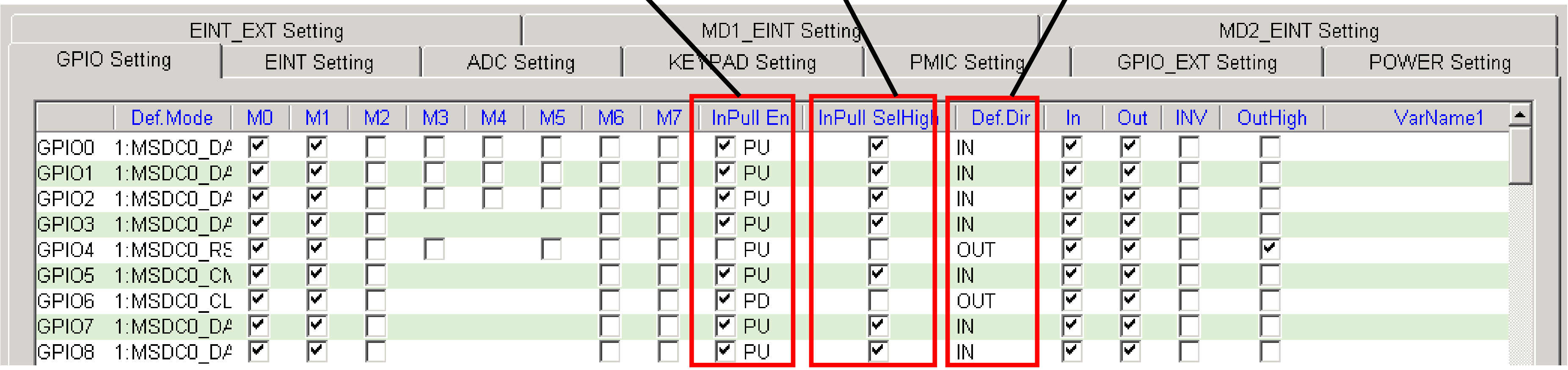
Design Notice – GPIO selection (3/x)

Notice of Drv_Tool usage

After enable “InPull En”, you can change the PU/PD value by changing “InPull SelHigh”.
(Only valid when GPIO is input mode)

“InPull En” can enable/disable PU/PD, then GPIO will be the default PU/PD value after reset state.
(Only valid when GPIO is input mode)

“OutHigh” can change the default output level.
(Only valid when GPIO is output mode)



	Def.Mode	M0	M1	M2	M3	M4	M5	M6	M7	InPull En	InPull SelHigh	Def.Dir	In	Out	INV	OutHigh	VarName1
GPIO0	1:MSDC0_DA	☑	☑	☐	☐	☐	☐	☐	☐	☑ PU	☑	IN	☑	☑	☐	☐	
GPIO1	1:MSDC0_DA	☑	☑	☐	☐	☐	☐	☐	☐	☑ PU	☑	IN	☑	☑	☐	☐	
GPIO2	1:MSDC0_DA	☑	☑	☐	☐	☐	☐	☐	☐	☑ PU	☑	IN	☑	☑	☐	☐	
GPIO3	1:MSDC0_DA	☑	☑	☐				☐	☐	☑ PU	☑	IN	☑	☑	☐	☐	
GPIO4	1:MSDC0_RS	☑	☑	☐	☐		☐	☐	☐	☐ PU	☐	OUT	☑	☑	☐	☑	
GPIO5	1:MSDC0_CN	☑	☑	☐				☐	☐	☑ PU	☑	IN	☑	☑	☐	☐	
GPIO6	1:MSDC0_CL	☑	☑	☐				☐	☐	☑ PD	☐	OUT	☑	☑	☐	☐	
GPIO7	1:MSDC0_DA	☑	☑	☐				☐	☐	☑ PU	☑	IN	☑	☑	☐	☐	
GPIO8	1:MSDC0_DA	☑	☑	☐				☐	☐	☑ PU	☑	IN	☑	☑	☐	☐	

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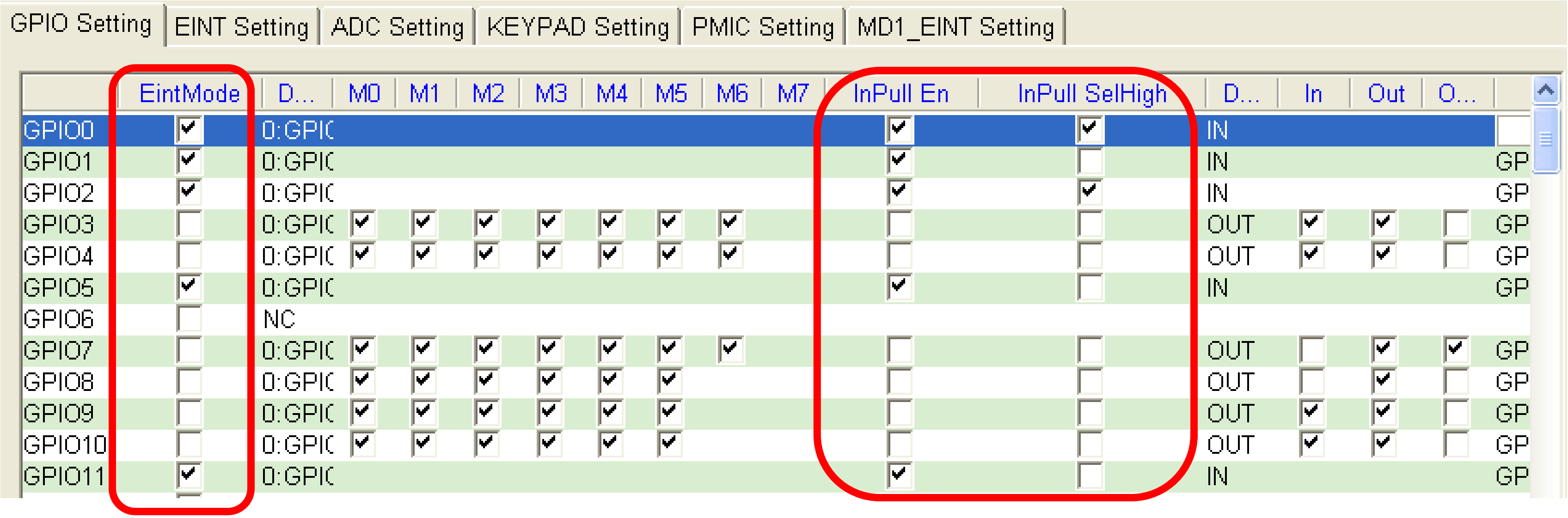
Design Notice – GPIO selection (4/x)

- **MT8127 have no dedicated EINT MUX mode.**
  - **New design, each GPIO (exclude GPIO12/13) can be configured as "External interrupt mode"**
  - **Please click EintMode in DCT tool for External Interrupt application**
  - **After choose EintMode, this pin is limited as interrupt usage**
  - **You can set pull-up or pull-down in "InPullEn" & "InPull SelHigh"**



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Design Notice – GPIO selection (5/x)

- **MT8127 voltage IO Overview**

No.	Power Domain	Application	PMIC Suggest IO Power Connection
1	DVDD28_DPI	GPIO_1V8	VIO18
2		DPI Interface	VEMC_3V3
3	DVDD28_NFI	GPIO_1V8	VIO18
4		MLC NAND	VEMC_3V3
5	DVDD28_MSDC0	eMMC	VIO18
6		MLC NAND	VEMC_3V3
7	DVDD28_MSDC1	1st T-Card, embedded SD	VMC
8		GPIO_2V8	VIO28
9		GPIO_1V8	VIO18
10	DVDD28_MSDC2	GPIO_3V3	VEMC_3V3
11		GPIO_2V8	VIO28
12		GPIO_1V8	VIO18
13	AVDD33_USB	USB	VUSB

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Design Notice – GPIO selection (6/x)

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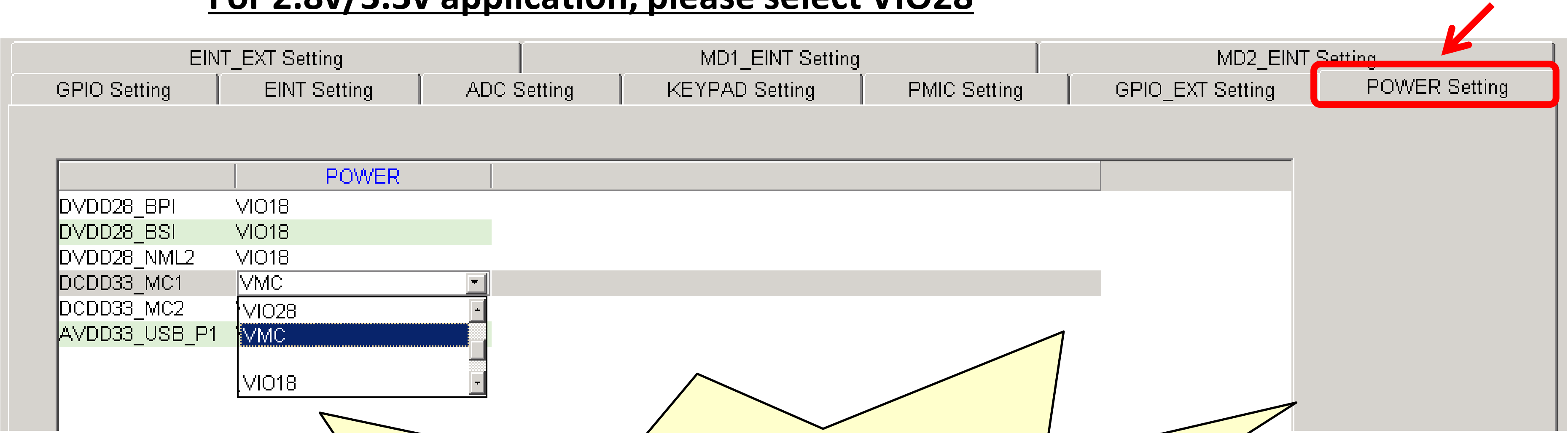
- **MT8127 High voltage IO DCT configuration**
  - **Define in DCT tool POWER Setting page**
  - **For 2.8v/3.3v application, please select VIO28**



Please review this item project by project
每個 Project 務必要 review 這頁設定以避免 IC IO 電壓錯誤而損毀

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Schematic Design Notice

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Schematic Notice – CPU/EMI Power (1/x)

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- EMI Power should follow MMD based on different PCB stack
- CPU Power should follow MMD or did PDN simulation
- VCCK, VCCK_VPROC has dedicated bulk power source from PMIC, **please do remote sense layout**
  - Power sense feedback from the bypass cap. close to MT8127

MT8127 CPU/EMI Power	PMIC Power source	PMIC Power remote sense pin
VCCIO	MT6397 VDRM (A17/A16)	MT6397 VDRM_FB (D15)
VCCK_VPROC	MT6397 VPCA15_1/VPCA15_2 (A6/A7/A4/A5)	MT6397 VPCA15_FB (E10) GND_VPCA15_FB (E11)
VCCK	MT6397 VCORE (A13/A14)	MT6397 VCORE_FB (D14)

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Schematic Notice – CPU/EMI Power (2/x)

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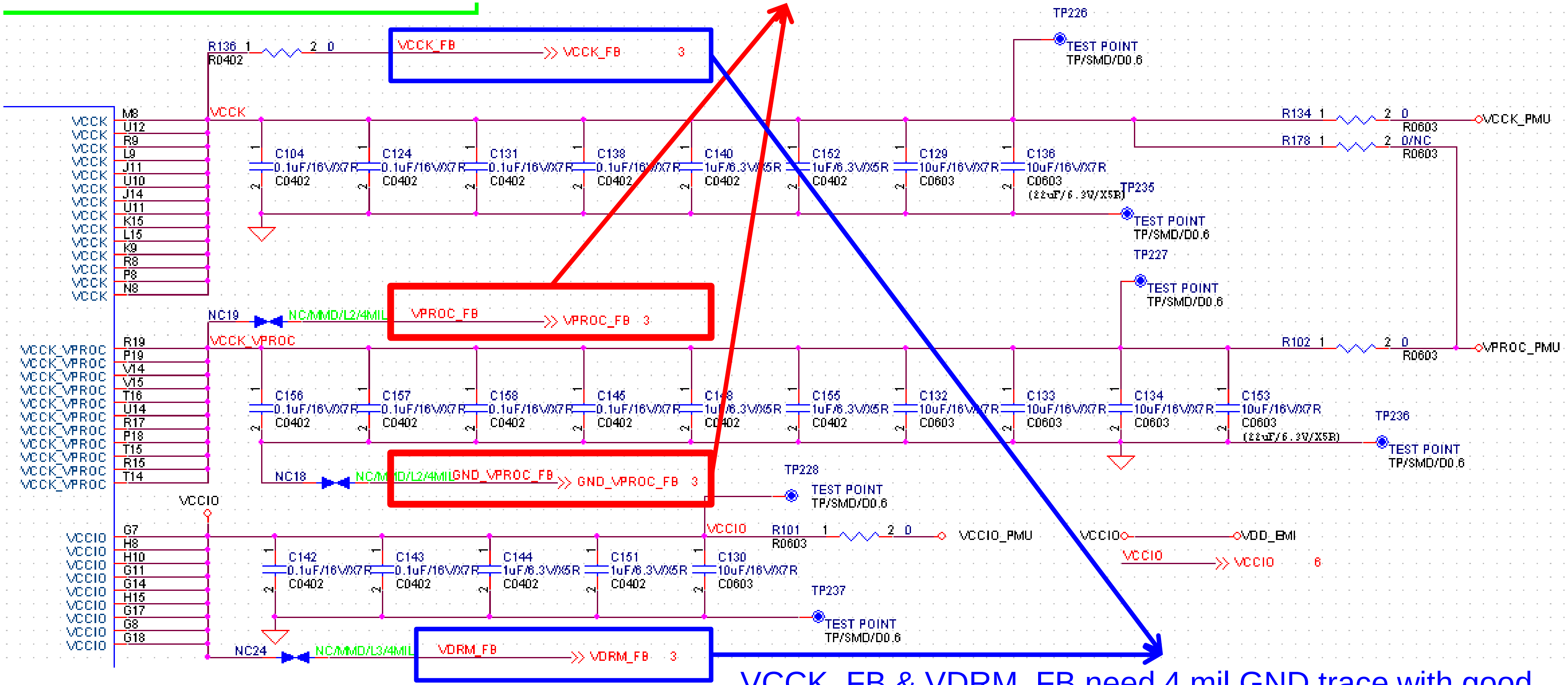
- CPU power VCCK_VPROC has dedicated bulk power source from PMIC MT6397, and POWER/GND pairs remote sense is applied to improve CPU performance

VPROC_FB /GND_VPROC_FB need differential routing and 4 mil GND trace with good shielding to PMIC



VCCK_FB & VDRM_FB need 4 mil GND trace with good shielding to PMIC

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Schematic Notice – Analog Power

Power domain	Power By	Bypass Cap.	Function
AVDD18_MEMPLL	VIO18 (MT6397)	0.1uF	DRAMC
AVDD18_AP	VIO18 (MT6397)	0.1uF	AUXADC, Temperature Sensor
AVDD18_PLLGP	VIO18 (MT6397)	0.1uF	PLL Group
DVDD18_MIPITX	VIO18 (MT6397)	0.1uF	MIPI DSI
DVDD18_MIPIRX	VIO18 (MT6397)	0.1uF	MIPI CSI
AVDD33_USB	VUSB (MT6397)	1uF	USB
AVDD18_USB	VIO18 (MT6397)	0.1uF	USB ; USB_PLL
AVDD18_HDMITX	VIO18 (MT6397)	0.1uF	HDMI

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Schematic Notice – General Power

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- High Speed IO bypass cap. should be high priority (Close to BB)
  - High Speed IO bypass cap. should put close to MT8127

Power Domain	Power By	IO Characteristic	Function	Bypass Cap.
DVDD28_MSDC0	VIO18 (MT6397)	High Speed	eMMC	0.1 uF
DVDD28_MSDC1	VMC (MT6397)	High Speed	1st T-Card/SDIO	0.1 uF
	VIO18 (MT6397)	Low Speed	GPIO with 1V8	
	VIO28 (MT6397)	Low Speed	GPIO with 2V8	
DVDD28_MSDC2	VIO18 (MT6397)	Low Speed	GPIO with 1V8	0.1 uF
	VIO28 (MT6397)	Low Speed	GPIO with 2V8	
DVDD28_NFI	VIO18 (MT6397)	Low Speed	GPIO with 1V8	0.1uF
	VIO28 (MT6397)		GPIO with 2V8	
	VEMC_3V3 (MT6397)	High Speed	MLC NAND I/F	
DVDD28_DPI	VIO18 (MT6397)	Low Speed	GPIO with 1V8	0.1uF
	VIO28 (MT6397)		GPIO with 2V8	
	VEMC_3V3 (MT6397)	High Speed	DPI I/F	
DVDD18_IO0	VIO18 (MT6397)	Low Speed	GPIO with 1V8	0.1 uF
DVDD18_IO1		Low Speed	GPIO with 1V8	0.1 uF
DVDD18_IO2		Low Speed	GPIO with 1V8	0.1 uF
DVDD18_IO3		Low Speed	GPIO with 1V8	0.1 uF

Schematic Notice – EINT

- MT8127 support x143 EINTs
  - Each GPIO (**exclude GPIO12/13**) can be configured as "External interrupt mode"
- Only EINT[0:11/14/15] supports HW de-bounce

EINT Ports	De-bounce	De-bounce Time
EINT [0:11/14/15]	HW based	0.5/1/16/32/64/128/256/512 ms
EINT [16:168]	SW based	1/16/32/64/128/256/512 ms

More Detail please reference to "MT8127 GPIO Table"

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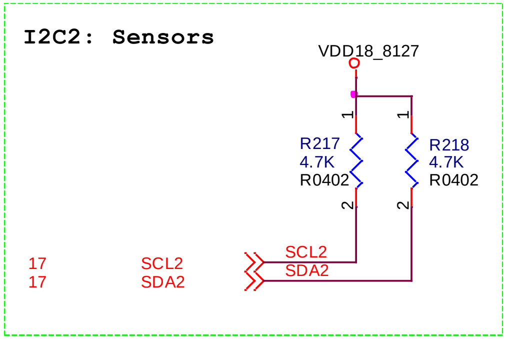
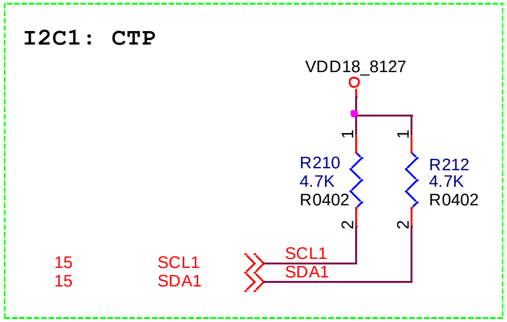
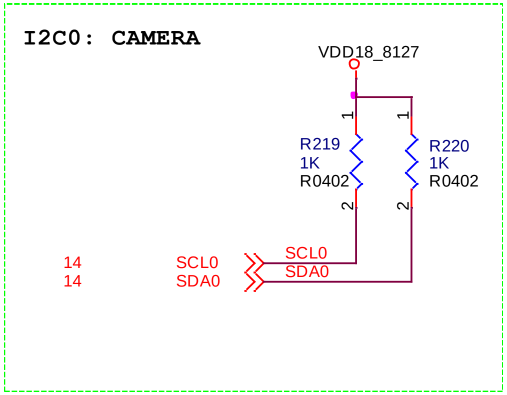
Schematic Notice – I2C

- MT8127 has x3 I2C controllers
  - I2C over MT8127
    - 3 dedicated I2C ports (I2C 0~2) with Open Drain IO design (Pull high resistor is need)

Pin Num	IO Reset default mode	Pin Name	Mode 0	Mode 1
W3	PU	SDA0	GPIO75	B1:SDA0
W4	PU	SCL0	GPIO76	B1:SCL0
AE23	PU	SDA1	GPIO57	B1:SDA1
AD23	PU	SCL1	GPIO58	B1:SCL1
K19	PU	SDA2	GPIO77	B1:SDA2
K20	PU	SCL2	GPIO78	B1:SCL2







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Schematic Notice – AUXADC

- MT8127 has x6 AUXADC ports
  - Input range support max. 1.45v
  - 12 bit resolution
- For thermal sensor's accuracy, the ADC reference voltage is 1.45V from internal (Not 1.8V in old platform). So the ADC input range is 1.45V only

MT8127 AUXADC Port	IO Domain	GPIO	Input Range	Resolution	Sampling Rate
AUX_IN0	AVDD18_AP	-	1.45v	12bit	3.25/(N+4) MSPS @ N-bit
AUX_IN1	AVDD18_AP	-	1.45v	12bit	3.25/(N+4) MSPS @ N-bit
AUX_IN2	AVDD18_AP	-	1.45v	12bit	3.25/(N+4) MSPS @ N-bit
AUX_IN3	AVDD18_AP	-	1.45v	12bit	3.25/(N+4) MSPS @ N-bit
AUX_IN4	AVDD18_AP	-	1.45v	12bit	3.25/(N+4) MSPS @ N-bit
AUX_IN5	AVDD18_AP	-	1.45v	12bit	3.25/(N+4) MSPS @ N-bit

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Schematic Notice – EFUSE Mode selection

Pin name	Pin	w/o EFUSE program	w/i EFUSE program
DVDD18_EFUSE	K7	GND	MT6397 VGP5 (2.0v)
FSOURCE_P	K8	GND	MT6397 VGP5 (2.0v)

Pin name	Pin out	Normal mode	TEST mode
MT6397_PMU_TESTMODE	D16	GND	VBAT
MT6397_FSOURCE	R2	GND (eFUSE DIS)	AVDD18_DIG (eFUSE EN)

•MT8127 eFUSE enable voltage need to 2.0v (PMIC general LDO VGP5)

• For normal usage, please configure above pins to be “Normal mode”.

•TESTMODE, are only for debugging, please follow above configuration.

•FSOURCE, are only for eFUSE , please follow above configuration.

•MT8127 eFUSE enable voltage need to 2.0v (PMIC general LDO VGP5)

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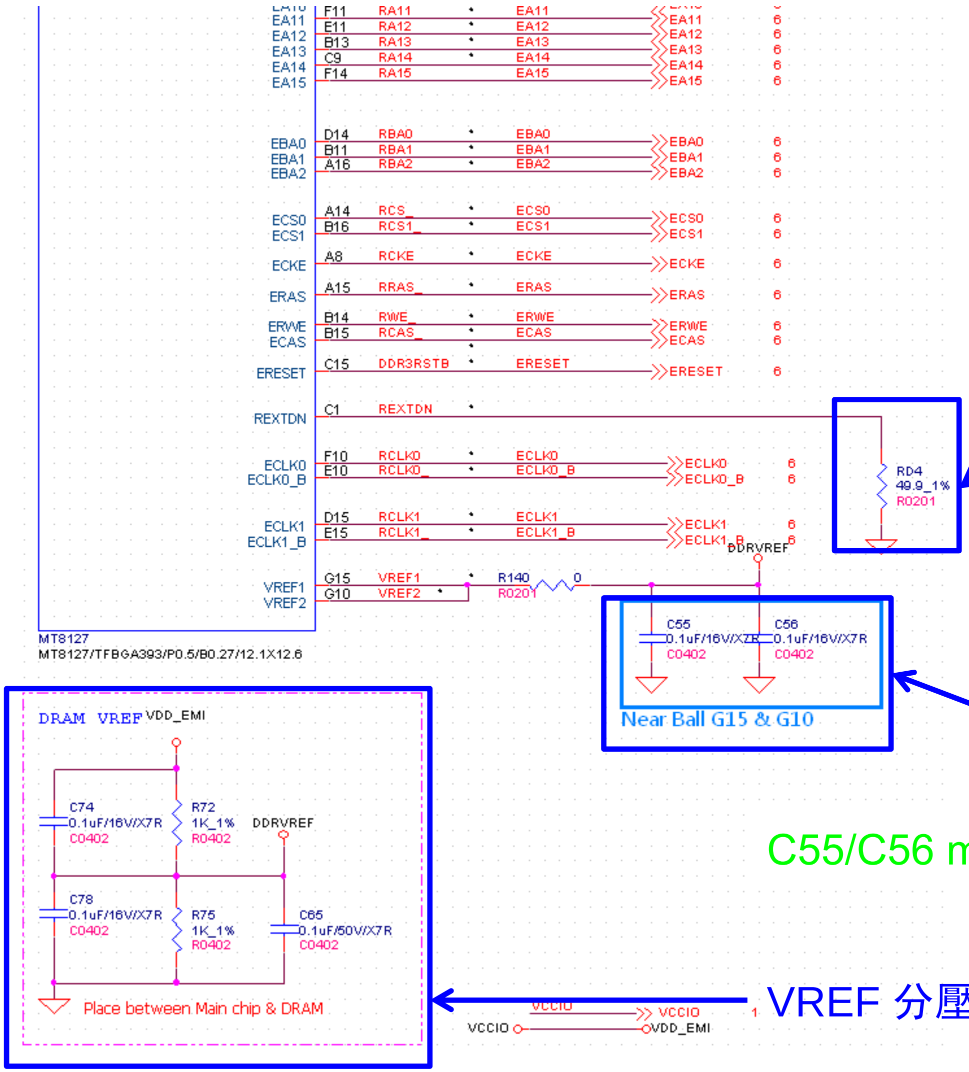
Schematic Notice – DRAM Application



REXTDN use 49.9_1% ohm resistor
For DRAM timing calibration

Pin name	Pin out	Voltage
VREF	G14/G12	½ DRAM IO

C55/C56 must place near Ball “G15” & “G10”

VREF 分壓電路請Follow MTK reference circuit

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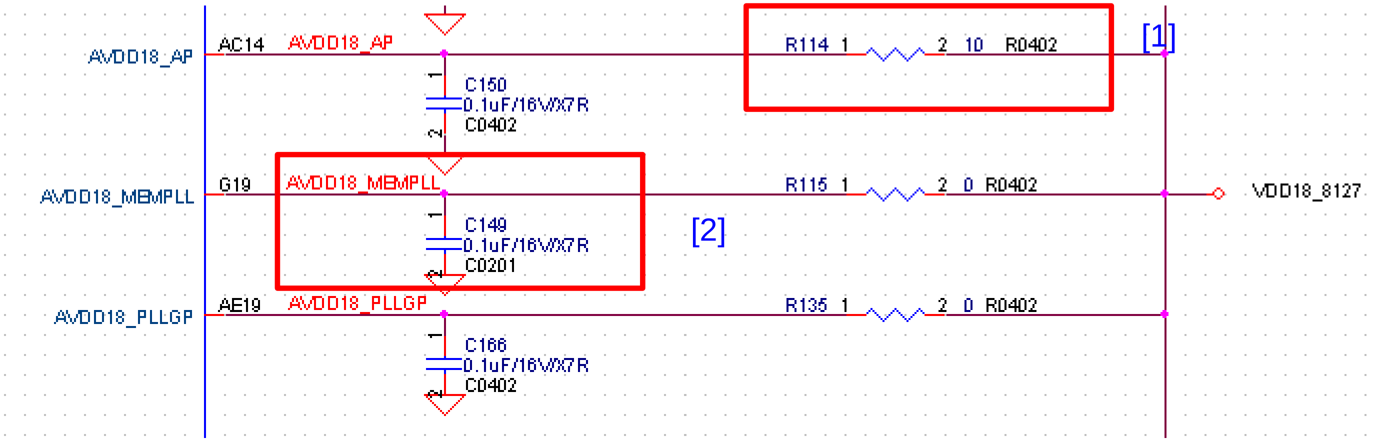
Schematic Notice – Analog power



- AVDD18_AP: Please reserve 10 ohm resistor on AVDD18_AP power path to improve power quality.[1]
- AVDD18_MEMPLL: C149 must close to MT8127 main chip <150 mil. [2]

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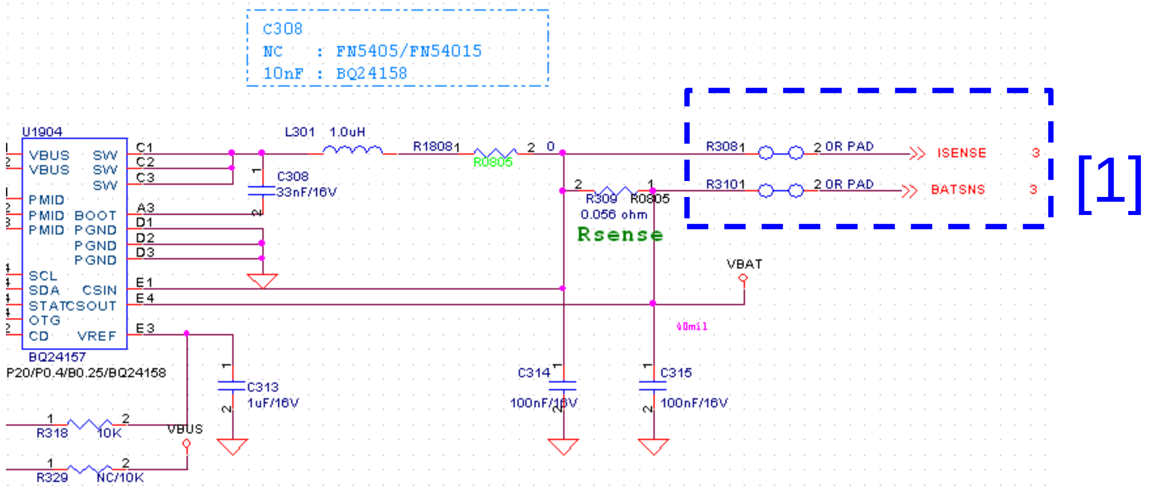
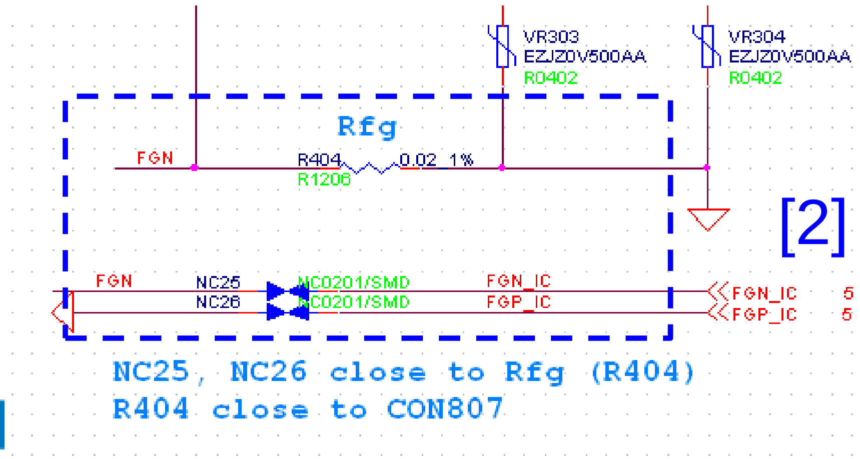
Schematic Notice – Charger

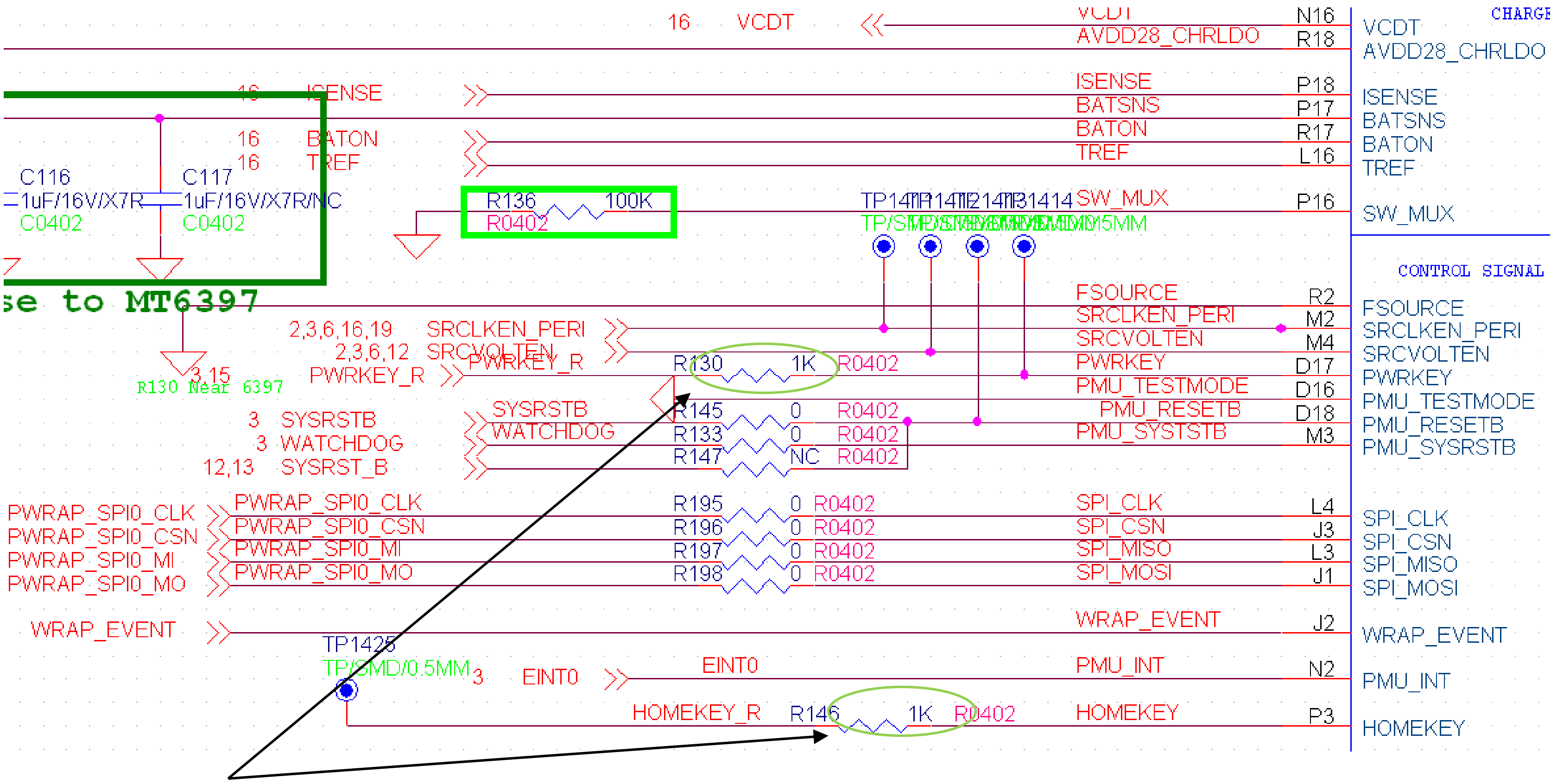
- Keep differential routing for ISENSE and BATSNS to Rsense [1]



•Keep differential routing for FGP and FGN to Rfg [2]



Schematic Notice – PWRKEY / HOMEKEY



Add a 1k Ohm resistor to avoid ESD damage

DO NOT put pull-up resistor on PWRKEY / HOMEKEY

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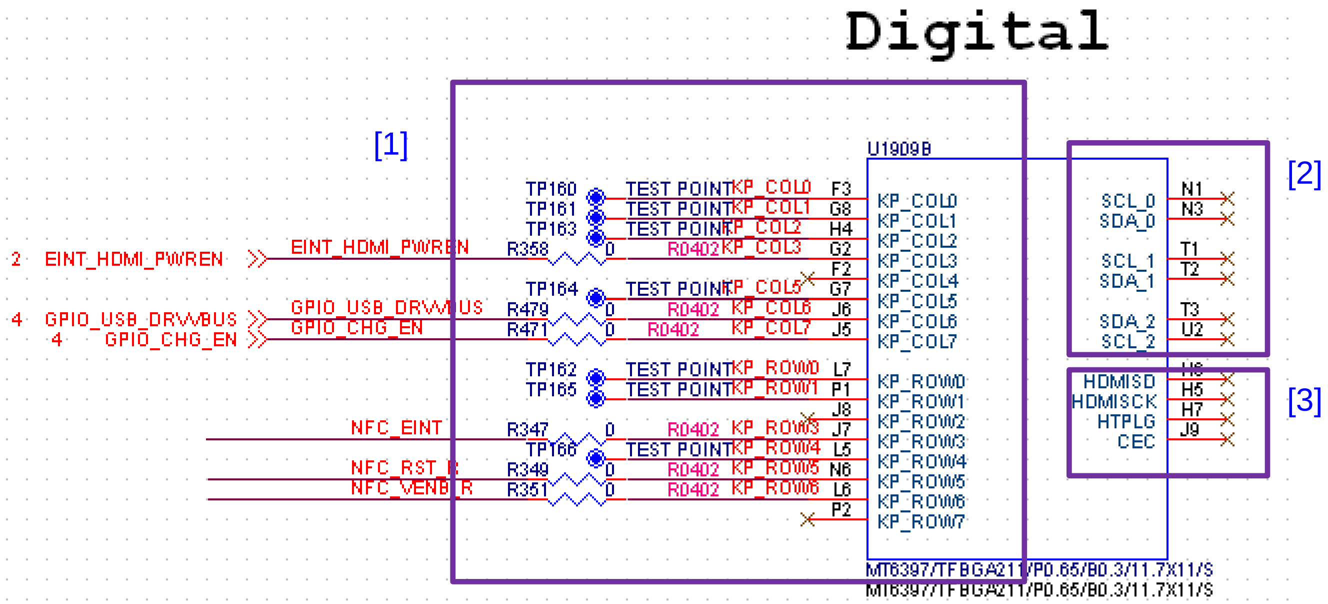
Schematic Notice – MT6397 PMIC [1/x]

- MT6397 has 16 pin key pad (KP_COL0~KPCOL7, KP_ROW0~KP_ROW7), but key function not support when using MT8127. These 16 pin only can be GPIO.[1]
- MT6397 has 3 sets I2C, but i2C function not support when using MT8127. These 6 pin only cab be GPIO.[2]
- MT6397 has 4 pin for HDMI digital (HDMISD/HDMISCK/HTPLG/CEC), but HDMI function not support. Please reserve these pins floating.[3]
- MT6397 has 41 pin GPIO (GPIO 0~GPIO40). Please notice these pins not support EINT function.



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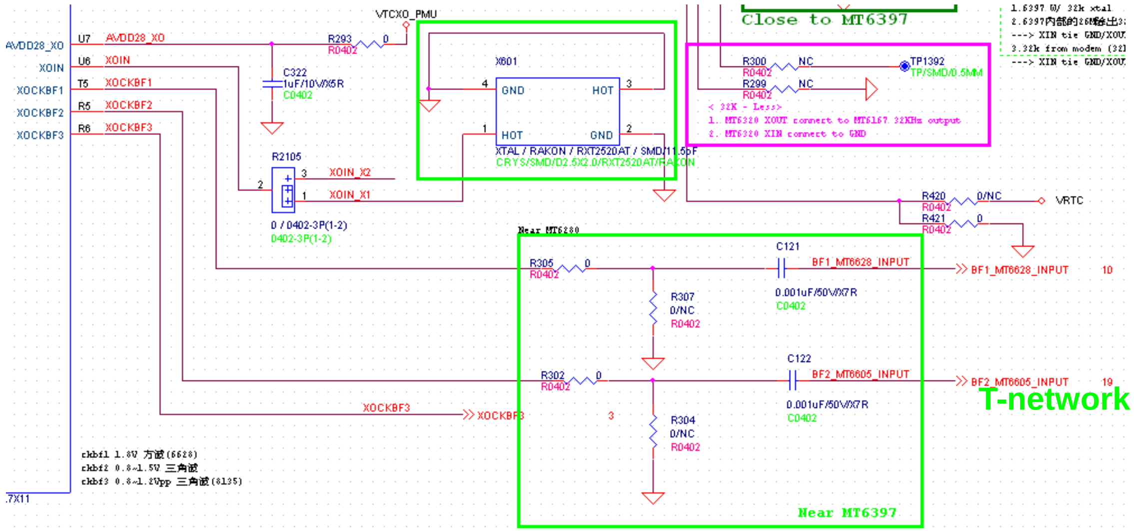
Schematic Notice – MT6397 PMIC [2/x]

- MT6397 support 3 set clock buffer output
- The clock arrangement must follow as below
  - XOCKBF1 is design for connectivity-MT6627 (note 1) (note 2) (note 3)
  - XOCKBF2 is design for NFC-MT6605 (note 2)
  - XOCKBF3 is design for AP-MT8127



NOTE1:MT6397 not support co-clock when MT6627 GPS function implement.
NOTE2:XOCKBF1& XOCKBF2 must reserve "T-network @ PMU side. =>Series 0R-Shunt NC-Series 10nF"
NOTE3:When co-clock w/ MT6627. 26M TCXO selection please follow "MT6627 26M TCXO QVL."

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Schematic Notice – MT6397 PMIC [3/x]

- **MT6397 26M XTAL Selection please follow MT6397 26M XTAL QVL**

Mediatek 26M Crystal for MT6397

Component	Part Number	Manufacturer	Vendor
X'TAL 2520	8Z26000054 (CL=11pF)	TXC	TXC
X'TAL 2520	IDD11RSX-10 26.000 MHz (CL= 11pF)	Rakon	Rakon

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MT8127 SD_eMMC Design Note

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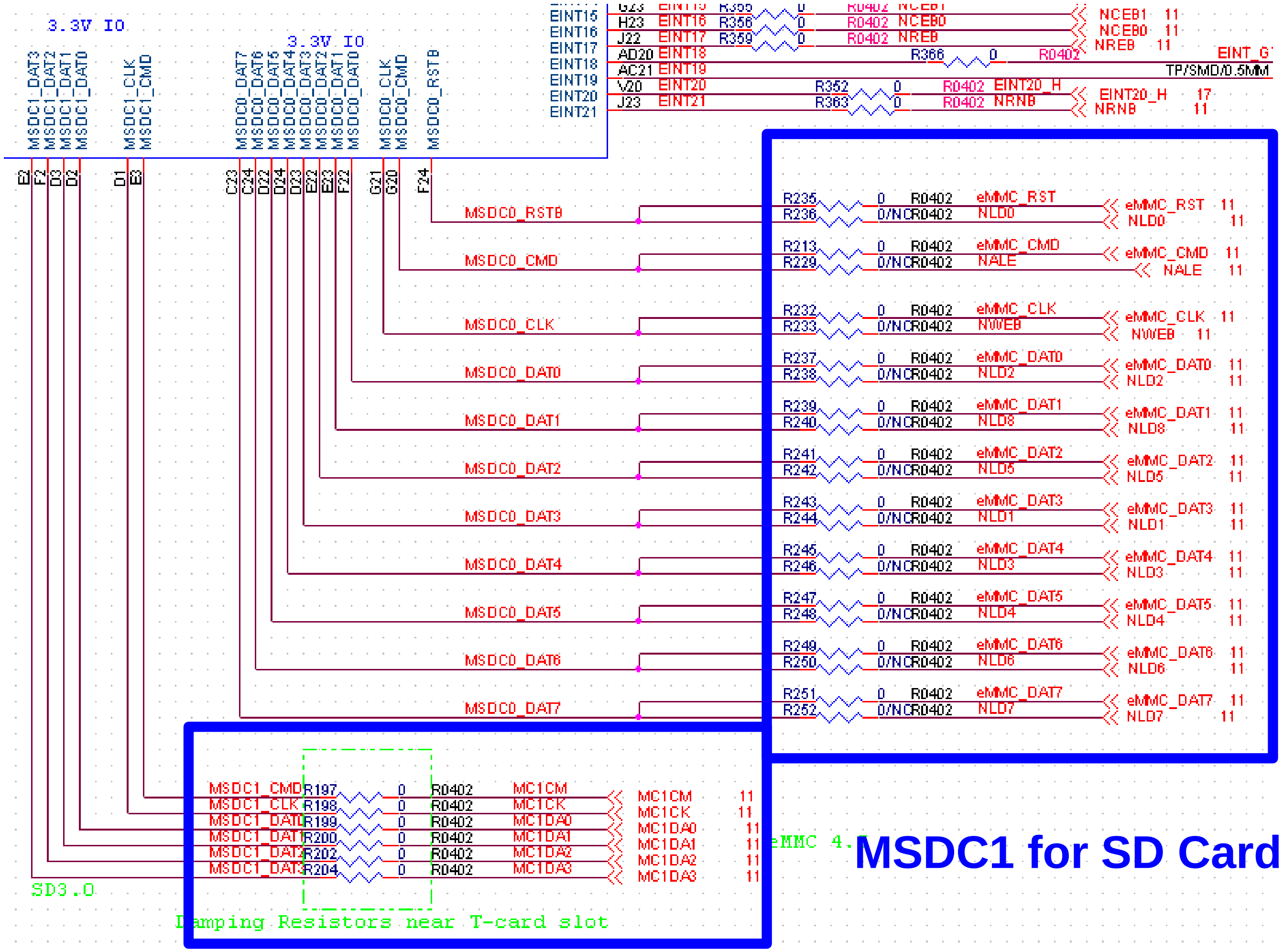
MT8127 MSDC HW Configuration



MSDC0 for eMMC or MLC NAND

MSDC1 for SD Card

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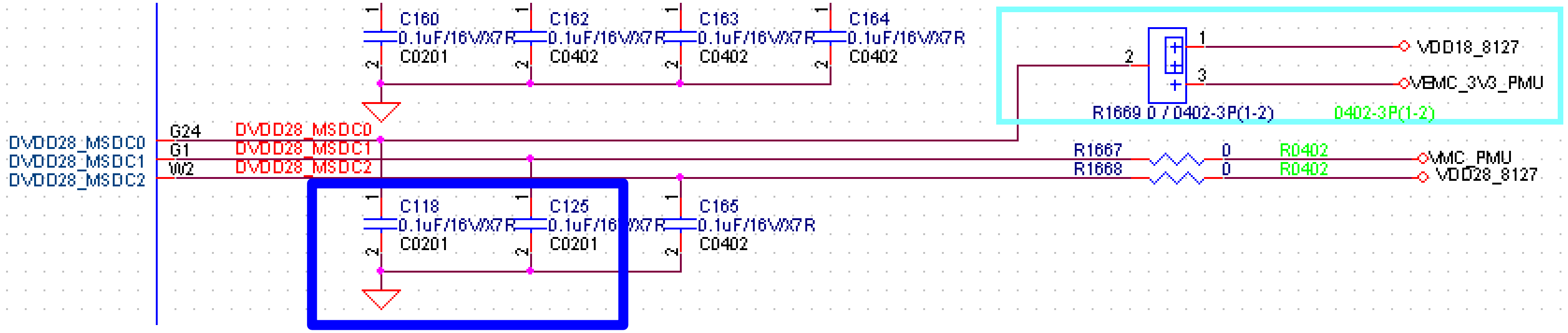
MT8127 MSDC I/O Pad Power

- The C118/C125 must close to G24 and G1 . The trace length limit is 150mil.(Must)



MT6397	default on ?	Voltage	Max. Current (mA)
VIO18	Y	1.8V	600
VMC	Y	1.8V / 3.3V	200
VMCH	Y	3.0V / 3.3V	800
VEMC_3V3	Y	3.0V / 3.3V	400

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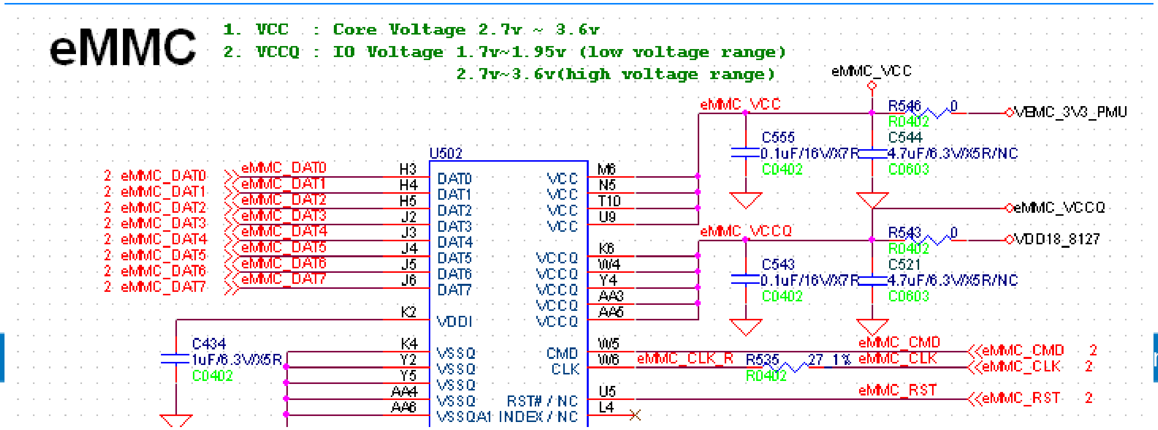
MT8127 8-bit eMMC (Using MSDC0 interface)

- eMMC_RST is mandatory for eMMC booting .(Must)
- Reserve a damping resistor position on the CLK interface
    - Check eMMC data sheet for the resistor value .(conditional)
- eMMC core power (VCC) should be 3.3V.(Must)
    - Suggest to use MT6397 VEMC_3V3 for eMMC VCC
    - Check the eMMC data sheet for the capacitor value.
- eMMC I/O power (VCCQ) should be 1.8V .(Must)
    - 1.8V power with 100mA capability is necessary
    - Suggest to use MT6397 VIO_18
    - Check the eMMC data sheet for the capacitor value.



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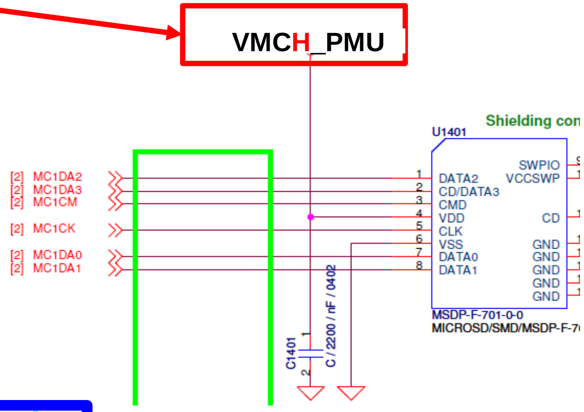
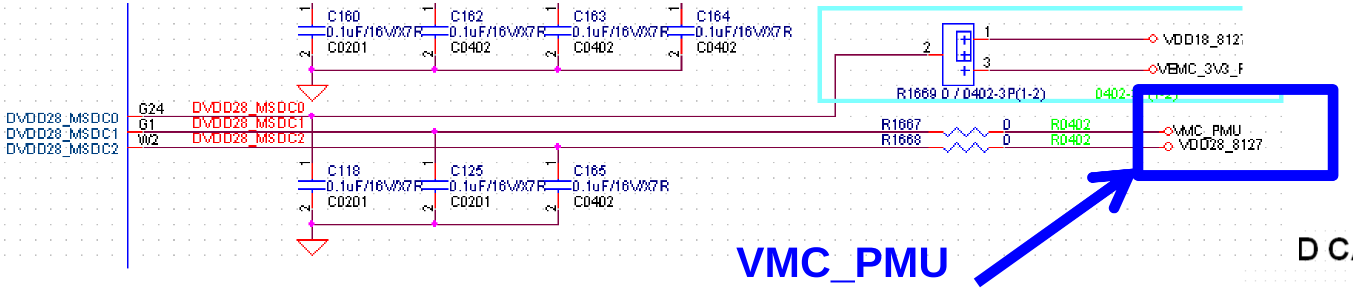
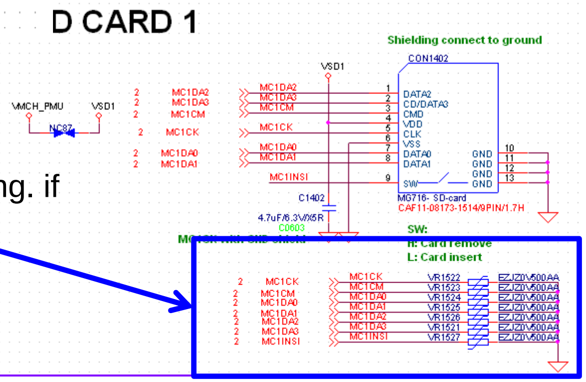
MT8127 MSDC1, SD 3.0 T-Card

- for SD 3.0 (SDR50/DDR50) application: (must)
  - 3.3V/400mA is necessary. VMCH for the SD card.
  - 3.3V/1.8V switchable VMC for the MT8127 (DVDD28_MSDC1).



- for SD 3.0 (SDR104) application: (must)
  - The 3.3V/800mA is necessary . VMCH for the SD card.
  - 3.3V/1.8V switchable VMC is for MT8127 (DVDD28_MSDC1).





- EMI /ESD protection device on CMD/CLK/DAT with Cap < 5pF
- Reverse the damping resistor position on the CLK, CMD, DAT to fine tune the AC timing. if the CLK, CMD, DAT trace length is less than 2000mils, the damping resistor can be removed.

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MT8127 MLC NAND I/F Design Note

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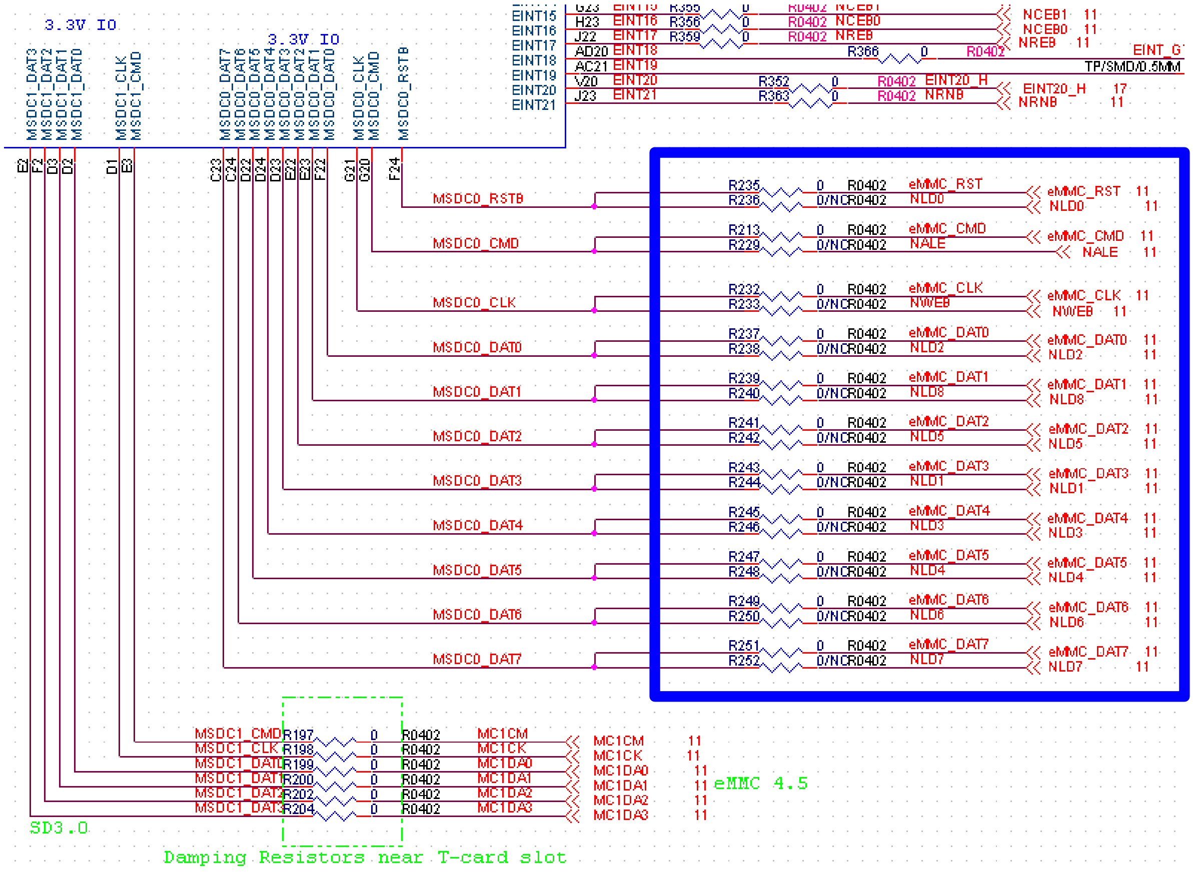
MT8127 MLC NAND I/F (1/2)

- MT8127 MLC I/F was pin-multiplexed with eMMC I/F (MSDC0)



MSDC0 for eMMC or MLC NAND

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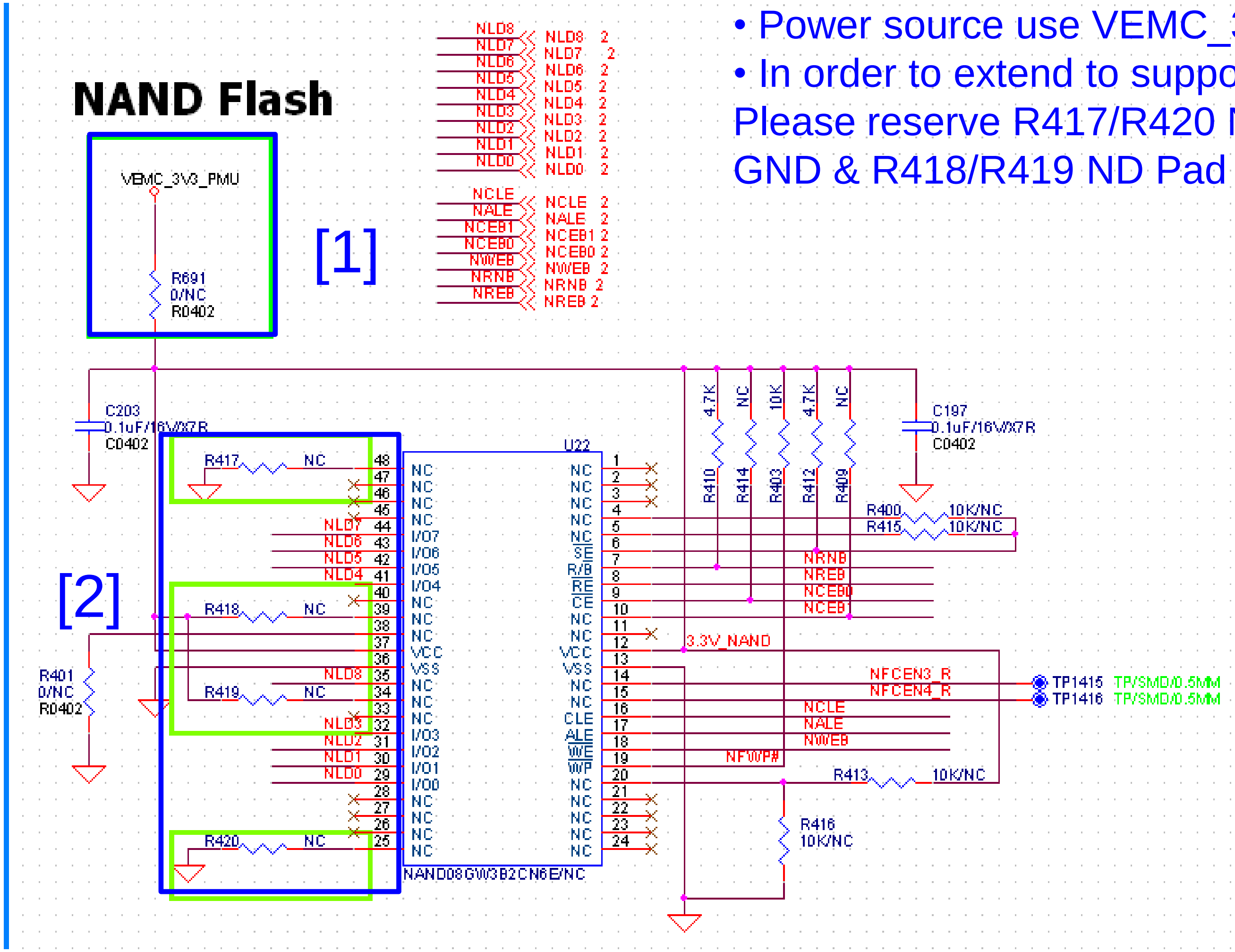
MT8127 MLC NAND I/F (2/2)

- MT8127 support 8 bit MLC NAND IF

- MLC NAND is 3.3V Device.
- Power source use VEMC_3V3 [1]
- In order to extend to support toggle NAND. Please reserve R417/R420 NC Pad short to GND & R418/R419 ND Pad short to VDD.[2]



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MT8127 USB 2.0 Design Notice

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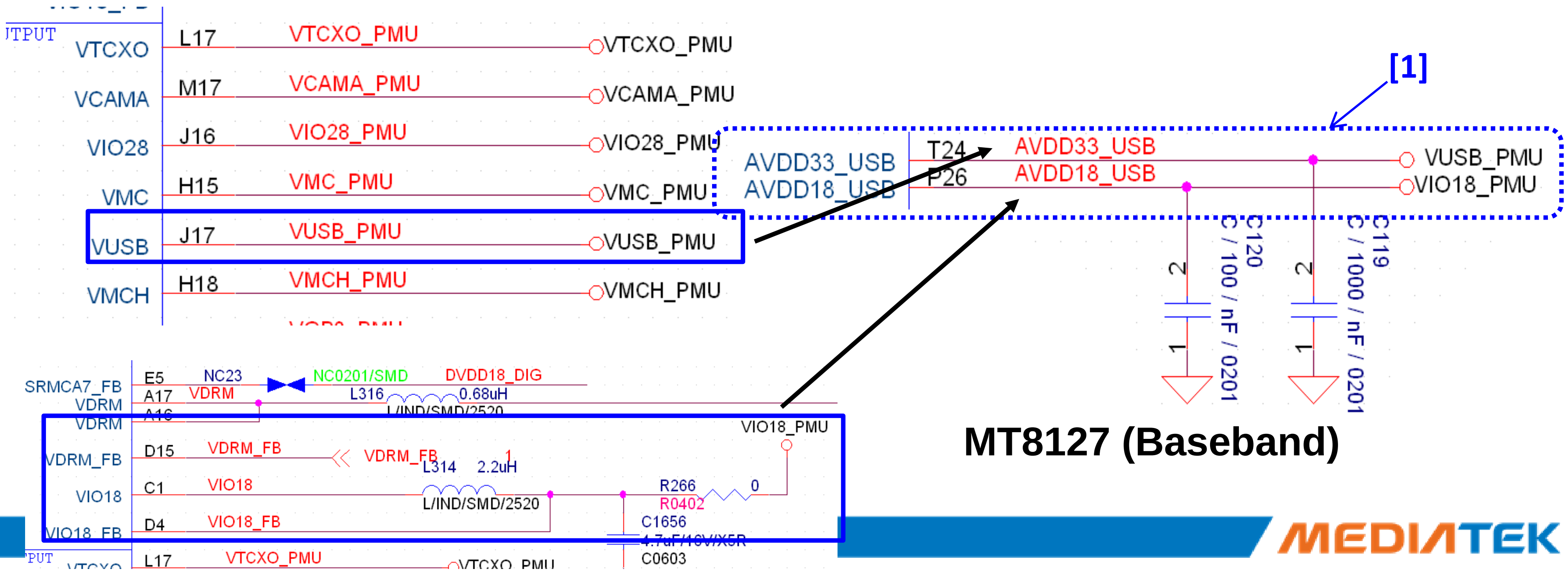
Schematic Notice – USB (1/x)

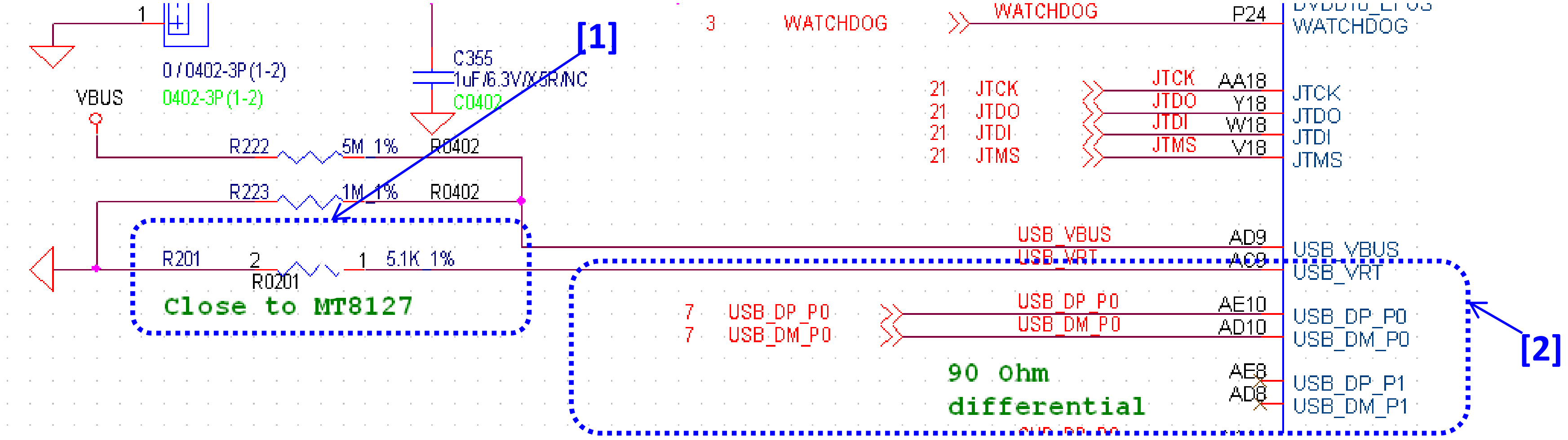
- MT8127 USB Power supply
  - USB Power
    - **3.3V power name:** AVDD33_USB. [1]
      - "AVDD33_USB" is powered by LDO "VUSB" of PMU for typical USB application.
      - To reserve de-coupling capacitor.
    - **1.8V power name:** AVDD18_USB. [1]
      - "AVDD18_USB " is powered by LDO "VIO18" of PMU for typical USB application.
      - To reserve de-coupling capacitor.

(PMIC) Side



Schematic Notice – USB (2/x)

- MT8127 USB schematic (1/3)
  - USB_VRT: 5.1K reference resistor for USB PHY reference current source. [1]
    - The USB_VRT resistor must be 5.1K-Ohm and with 1% precision.
    - The USB_VRT resistor must be placed as close to main chip's USB_VRT ball as possible in PCB layout.
    - Be aware of USB_VRT pin and it's trace routing should keep away from noise source and high speed clock data like camera data bus.
  - USB Differential pair: USB_DM/ USB_DP. [2]
    - The USB 90-Ohm characteristic impedance must be implemented in PCB layout.
    - The rating voltage of USB_DM/ USB_DP is 3.63V (3.3V+ 10%).



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Schematic Notice – USB (3/x)

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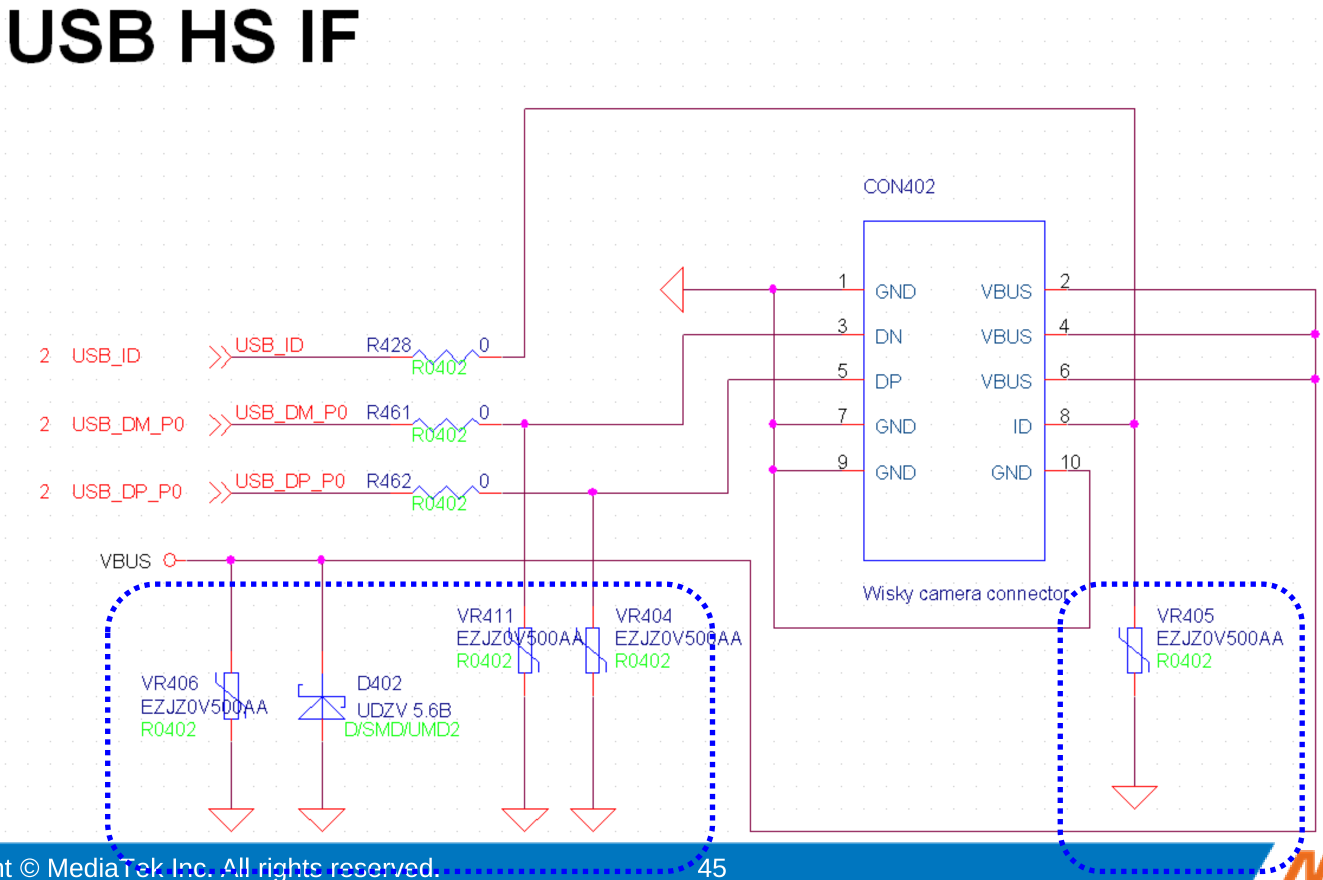
- MT8127 USB schematic (2/3)
  - USB application circuit on receptacle side
    - Place ESD protection device for USB differential pair and USB ID pin and VBUS pin.
    - The equivalent capacitance loading of ESD protection device should be less than 3pF.



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MT8127 HDMI/MHL Design Note

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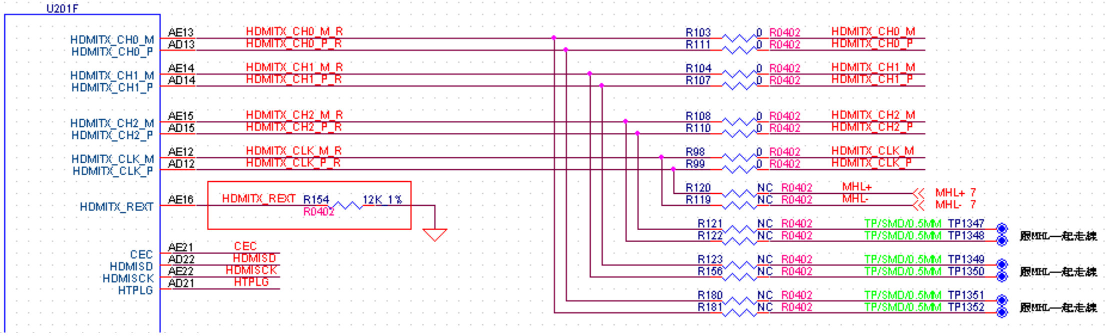
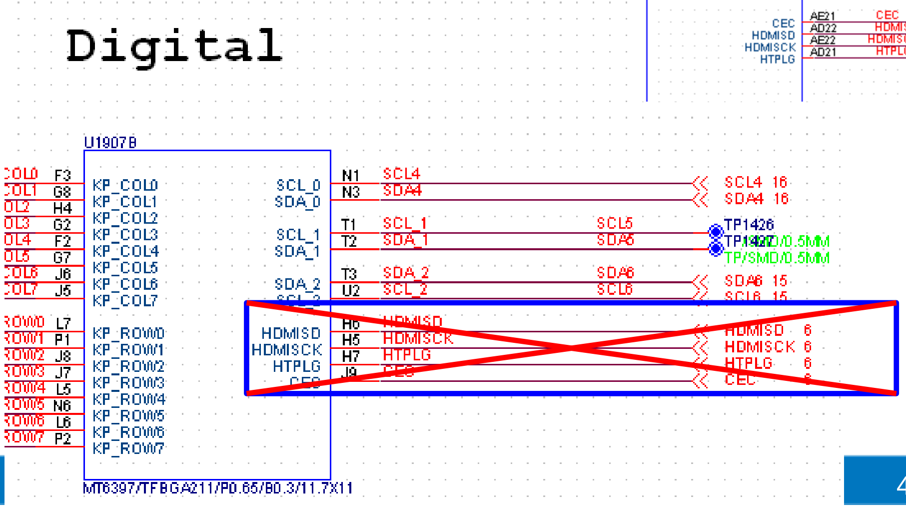
Schematic Notice – HDMI/MHL (1/x)

- MT8127 Built-in HDMI Tx 1.4a(3D)/MHL supports full HD 1080p video output.
- HDMI Multi-function w/ MHL IF, Pin mux table as below

Netname	Ball Location	HDMI	MHL
HDMITX_CLK_M	AE12	HDMITX_CLK_M	MHL-
HDMITX_CLK_P	AD12	HDMITX_CLK_P	MHL+

- HDMI_REXT resistor must use 12K_1%精密電阻
- HDMI DAT/CLK trace need 100 ohm impedance control





NOTE: Do not use HDMI DDC/ HTPLG/CEC control signal on MT6397 !!

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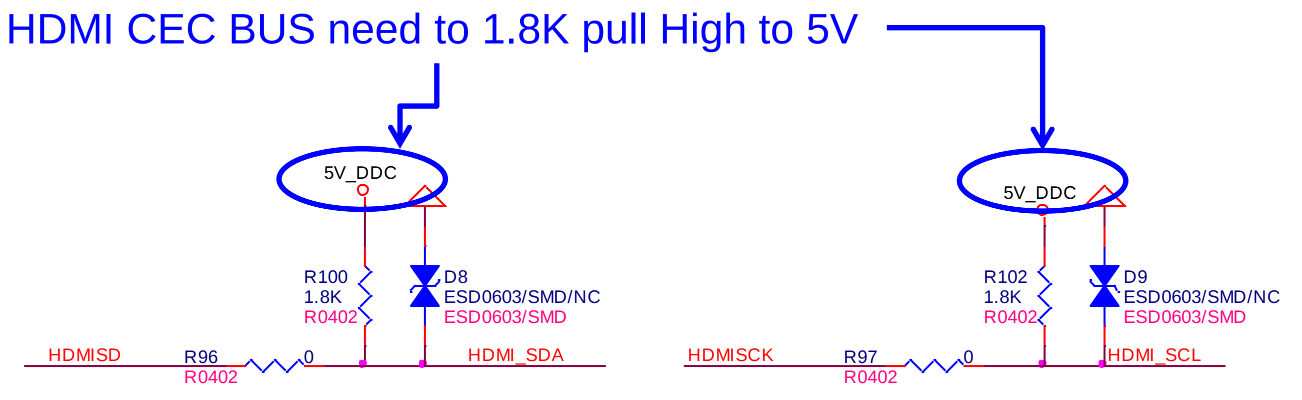
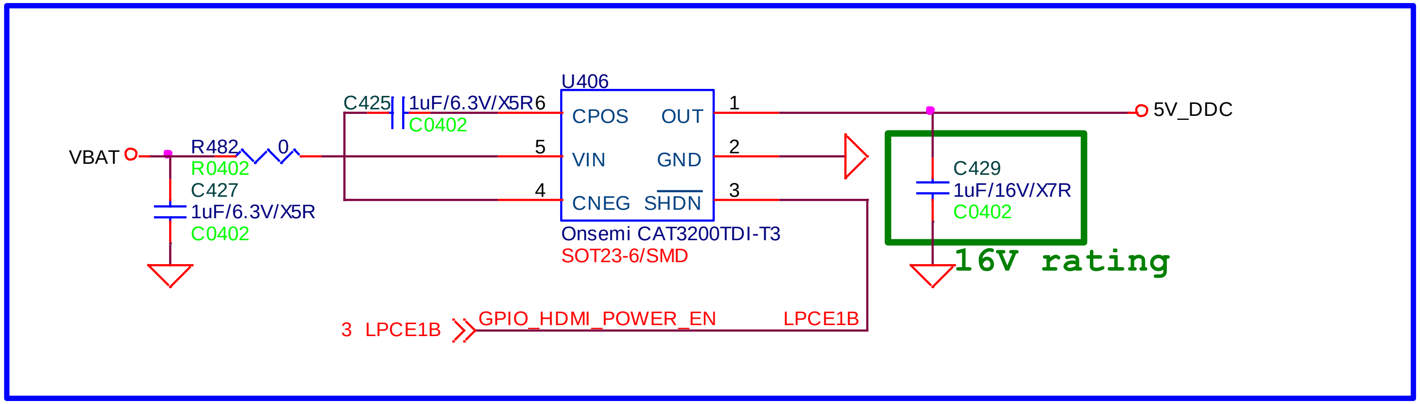
Schematic Notice – HDMI (2/x)



- Need add DC-DC to provide HDMI 5V.
- This DC-DC need have enable control pin to SHDN the 5V output power.



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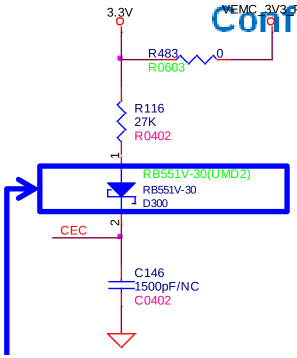
Schematic Notice – HDMI (3/x)

The Schottky Diode on CEC line Validation list



Please select qualified diode by MTK for passing HDMI test

Item	Vendor	Part Number	Verification status	PD(mW)	Package	Forward Voltage	IRM	Capacitance	contact window
1	Diodes	BAT54WS	Pass	200mW	SOD-323	400mV @ IF = 10mA	2.0uA @VR=25V	10pf @VR=1.0V,f=1.0MHz	Life Lee/李雪峰 Tel: 86-755-88284988 Ext: 662 Mobile: 139-2462-9451 Email: life_lee@cn.diodes.com
2	ROHM	RB751VM-40TE-17	Pass		SOD-323	370mV @ IF = 1mA	0.5uA @VR=30V	2pf @VR=1.0V,f=1.0MHz	吴金桂 Tel： 0755-8307-3008 Mobile： 13902998540 fouracewu@rohmsz.com.cn
3	Diodes	BO540WS-7	Pass	235mW	SOD-323	285mV @IF = 10mA	5uA @VR=30V	125pf @VR=0V,f=1.0MHz	Life Lee/李雪峰 Tel: 86-755-88284988 Ext: 662 Mobile: 139-2462-9451 Email: life_lee@cn.diodes.com
4	Semiconductor	SIG631E30T1G	Pass	200mW	SOD-523	500mV @IF=200mA	30uA @VR=10V	28pf @VR=0V， f=1MHz	
5	Diodes	BAT43WS	Pass	200mW	SOD-323	320mV @IF = 1mA	500nA @VR=25V	10pf @VR=1.0V,f=1.0MHz	Life Lee/李雪峰 Tel: 86-755-88284988 Ext: 662 Mobile: 139-2462-9451 Email: life_lee@cn.diodes.com
6	comchip	CDBF54-HF	Pass	200mW	SOD-323F	320mV @IF = 1mA	2.0uA @VR=25V	10pf @VR=1.0V,f=1.0MHz	典琦科技股份有限公司 Ada Wang 王雅芳 TEL:02-8677-6675 # 226 Mobil:0955 871 871

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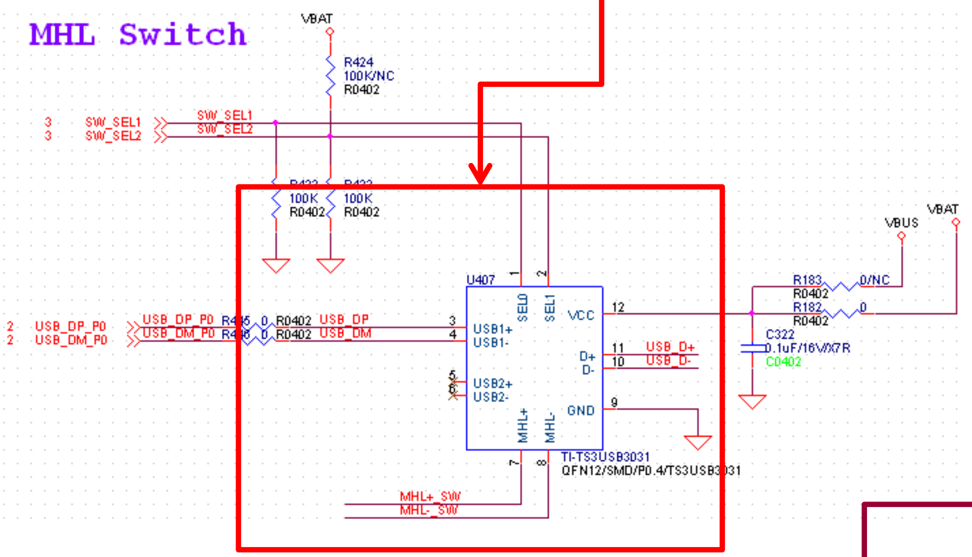
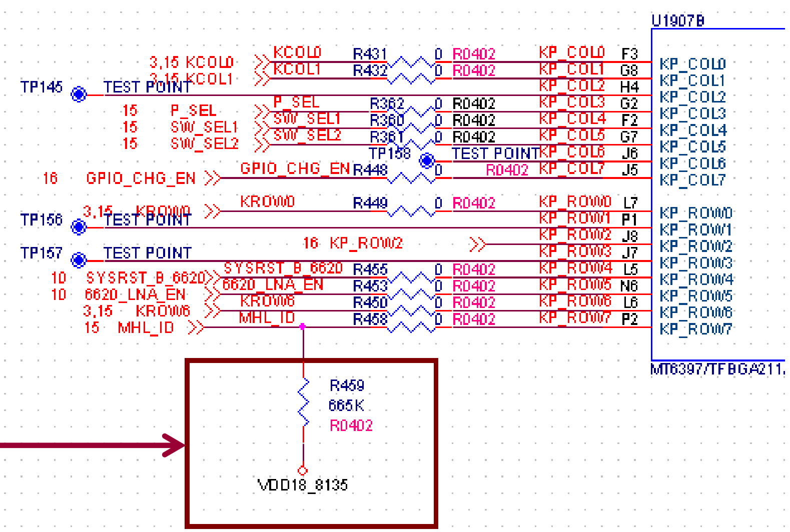
Schematic Notice – MHL (1/x)

MT8127 MHL IF is mux w/ HDMI, pin mux table as below

Netname	Ball Location	HDMI	MHL
HDMITX_CLK_M	AA12	HDMITX_CLK_M	MHL-
HDMITX_CLK_P	AB12	HDMITX_CLK_P	MHL+

- Need add a USB/MHL switch, this switch C load must <2 pF
- The switch default select to USB path





- The MHL ID Pin is Mux w/ MT6397 KP_ROW7.
- Need add a 665K pull up 1.8V Resistor.

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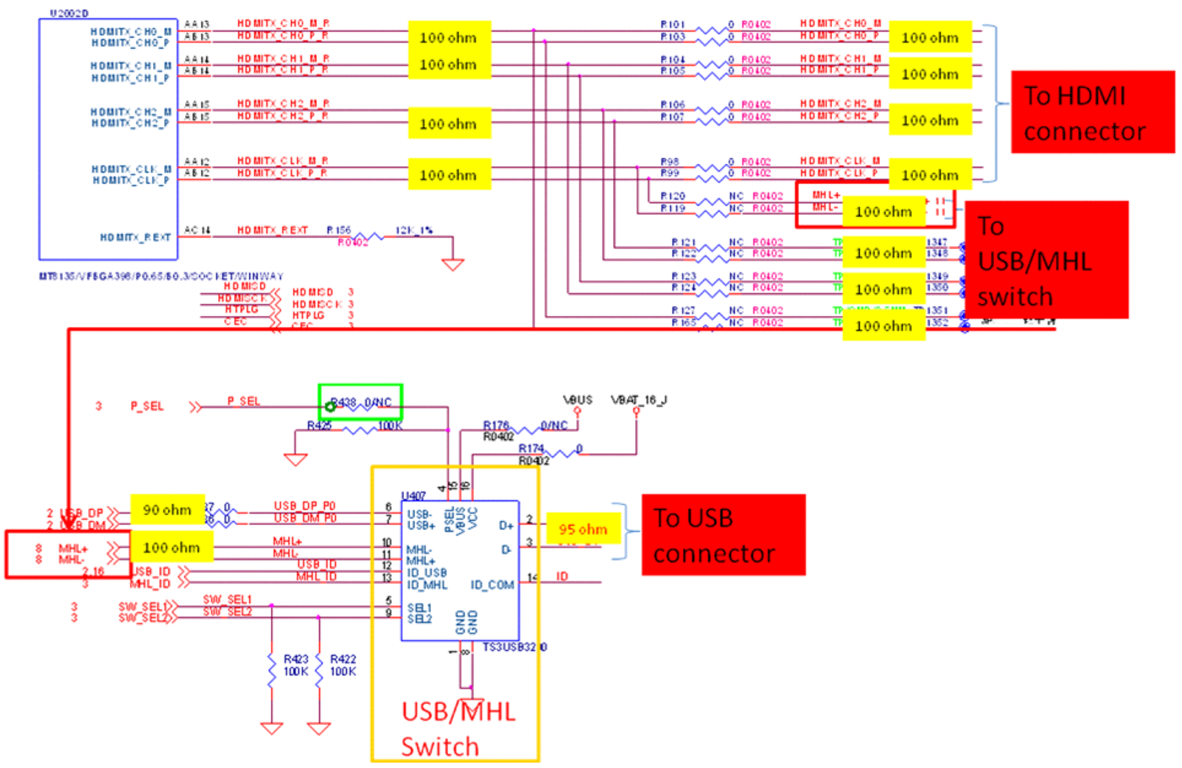
Schematic Notice – MHL

- MHL impedance control please reference to below picture
- MHL impedance control請務必遵守 **Zdiff = 100 Ω ± 15%, Zcom = 30 Ω ± 20%.**
- MHL to USB connector need 95 ohm impedance in order to match USB 90 ohm impedance spec.

MT8135 M1-V1 HDMI/MHL/USB impedance control 示意圖



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MT8127 Camera Design Notice

V0.1

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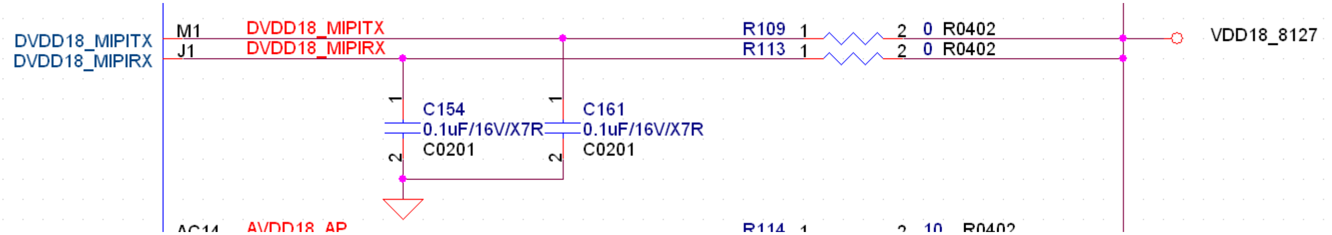
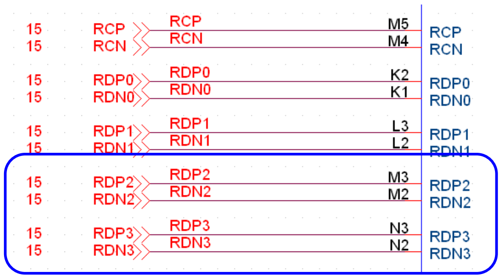
Schematic Notice – Camera (1/x)

- MT8127 Image Sensor Interfaces – MIPI "CSI-2" (1/2)
  - Power
    - **Power name:** DVDD18_MIPITX & DVDD18_MIPIRX.
      - Front-facing (Sub-camera) and Rear-facing camera (Main) camera interface is powered by DVDD18_MIPITX and DVDD18_MIPIRX.



  - MIPI "CSI-2" four-lane interface for rear-facing (main) camera
    - Differential pair of MIPI CSI, four-lane:
      - RCP / RCN.
      - RDP0 / RDN0; RDP1 / RDN1.
      - RDP2 / RDN2; RDP3 / RDN3.



    - The data lane number of MIPI "CSI-2" four-lane can be configured to support 1, 2 or 4 lane.
      - Signals to support 1~n data lane, where n= 4:
        { RCP / RCN } ; { RDP0 / RDN0 } to { RDP(n-1) / RDN(n-1) }
    - The data-lane-2 and data-lane-3 of MIPI CSI four-lane interface was pin-multiplexed with parallel interface (CM).
      - Only two data-lane can be supported for rear-facing camera when parallel interface be enabled.
    - The data receiving throughput of MIPI "CSI-2" four-lane interface can up to 1Gbps.

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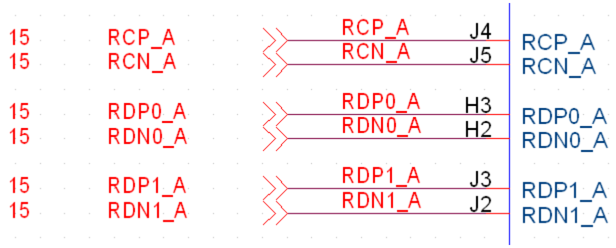
Schematic Notice – Camera (2/x)

- MT8127 Image Sensor Interfaces – MIPI "CSI-2" (2/2)
  - MIPI "CSI-2" two-lane interface for front-facing camera (Sub camera)
    - Differential pair of MIPI CSI, two-lane:
      - RCP_A / RCN_A
      - RDP0_A / RDN0_A
      - RDP1_A / RDN1_A



    - The data lane number of MIPI CSI two-lane can be 1 or 2.
      - Signals for 1 data lane: {RCP_A / RCN_A } ; {RDP0_A / RDN0_A }
      - Signals for 2 data lane: {RCP_A / RCN_A } ; {RDP0_A / RDN0_A } ; {RDP1_A / RDN1_A }
    - The MIPI CSI two-lane interface was pin-multiplexed with parallel interface (CM).
    - The data receiving throughput of MIPI CSI two-lane interface can up to 800Mbps.

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Schematic Notice – Camera (3/x)

- MT8127 Image Sensor Interfaces – Parallel 10-bit (1/2)
  - Parallel interface (CM) was pin multiplexed with MIPI CSI two-lane and the data-lane-2 and data-lane-3 of MIPI CSI four-lane interface.
    - CM signals
      - CMMCLK (MCLK)
      - CMPCLK (PCLK)
      - CMHREF (HSYNC)
      - CMVREF (VSYNC)
      - CMDAT[9:0] (10-bit data)
      - Power down pin for main camera
      - Reset pin for main camera.
      - Power down pin for Sub-camera.
      - Reset pin for Sub-camera
      - I2C-0
    - IO level is defined by "DVDD18_VIO"
    - Only CSI two-lane interface can be supported for rear-facing camera when parallel interface be enabled.

IO Power Domain	Pin Num	Pin Name	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3
DVDD18_MIPIRX	K1	PAD_RDN0	GPIO101	I:RDN0		
DVDD18_MIPIRX	K2	PAD_RDP0	GPIO102	I:RDP0		
DVDD18_MIPIRX	L2	PAD_RDN1	GPIO103	I:RDN1		
DVDD18_MIPIRX	L3	PAD_RDP1	GPIO104	I:RDP1		
DVDD18_MIPIRX	M4	PAD_RCN	GPIO105	I:RCN		
DVDD18_MIPIRX	M5	PAD_RCP	GPIO106	I:RCP		
DVDD18_MIPIRX	M2	PAD_RDN2	GPIO107	I:RDN2	I0:CMDAT8	
DVDD18_MIPIRX	M3	PAD_RDP2	GPIO108	I:RDP2	I0:CMDAT9	
DVDD18_MIPIRX	N2	PAD_RDN3	GPIO109	I:RDN3	I0:CMDAT4	
DVDD18_MIPIRX	N3	PAD_RDP3	GPIO110	I:RDP3	I0:CMDAT5	
DVDD18_MIPIRX	J5	PAD_RCN_A	GPIO111	I:RCN_A	I0:CMDAT6	
DVDD18_MIPIRX	J4	PAD_RCP_A	GPIO112	I:RCP_A	I0:CMDAT7	
DVDD18_MIPIRX	J2	PAD_RDN1_A	GPIO113	I:RDN1_A	I0:CMDAT2	I0:CMCSD2
DVDD18_MIPIRX	J3	PAD_RDP1_A	GPIO114	I:RDP1_A	I0:CMDAT3	I0:CMCSD3
DVDD18_MIPIRX	H2	PAD_RDN0_A	GPIO115	I:RDN0_A	I0:CMHSYNC	
DVDD18_MIPIRX	H3	PAD_RDP0_A	GPIO116	I:RDP0_A	I0:CMVSYNC	
DVDD18_IO2	G5	PAD_CMDAT0	GPIO117	I0:CMDAT0	I0:CMCSD0	O:ANT_SEL2
DVDD18_IO2	G4	PAD_CMDAT1	GPIO118	I0:CMDAT1	I0:CMCSD1	O:ANT_SEL3
DVDD18_IO2	F3	PAD_CMMCLK	GPIO119	O:CMMCLK		O:ANT_SEL4
DVDD18_IO2	G6	PAD_CMPCLK	GPIO120	I0:CMPCLK	I0:CMCSK	O:ANT_SEL5

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Schematic Notice – Camera (4/x)

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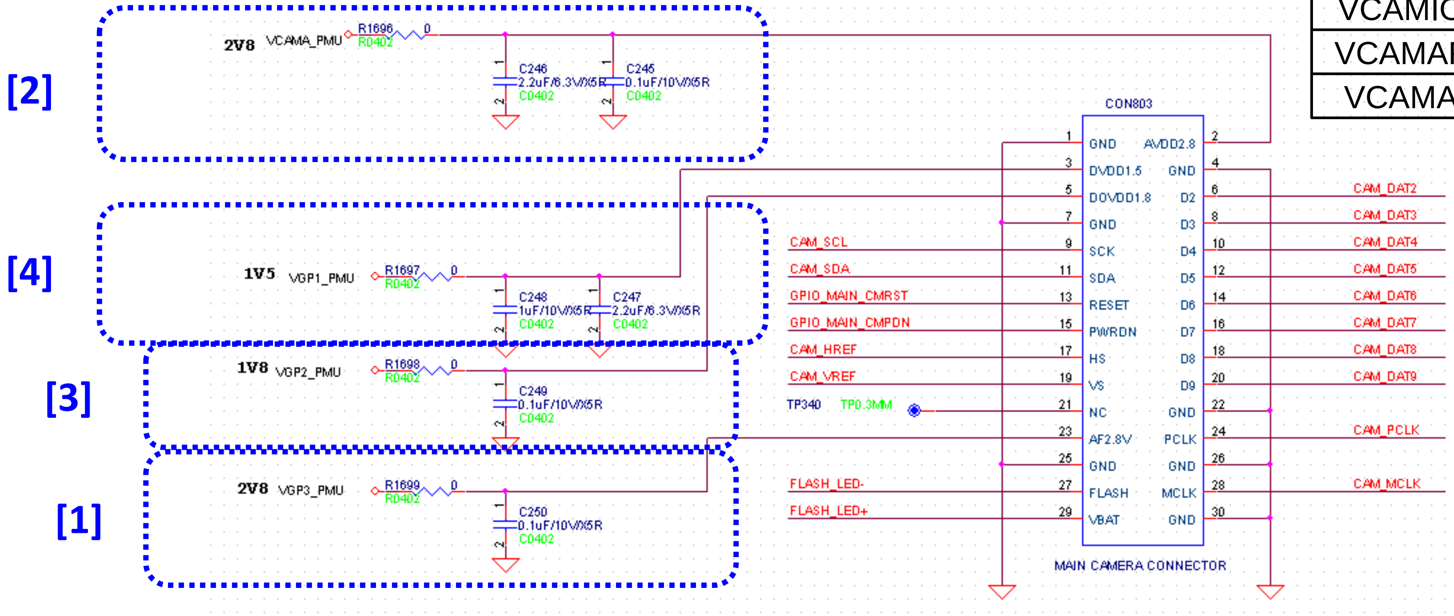
- Application circuit of rear facing camera
  - Power supply (1/2)
    - Auto focus (AF) 2.8V power of camera module is powered by PMU's VCAM_AF(VGP3_PMU). [1]
    - Analog 2.8V power of camera module is powered by PMU's VCAM_A. [2]
    - I/O 1.8V power of camera module is powered by PMU's VCAM_IO. [3]
    - Core power of camera module is powered by PMU's VCAM_D. [4]

MT6397	Max. Current (mA)
VCAMD	300
VCAMIO	200
VCAMAF	200
VCAMA	200



NOTE : Please check the voltage / current requirement of your selected camera sensor and compare with the relevant spec of their power source.

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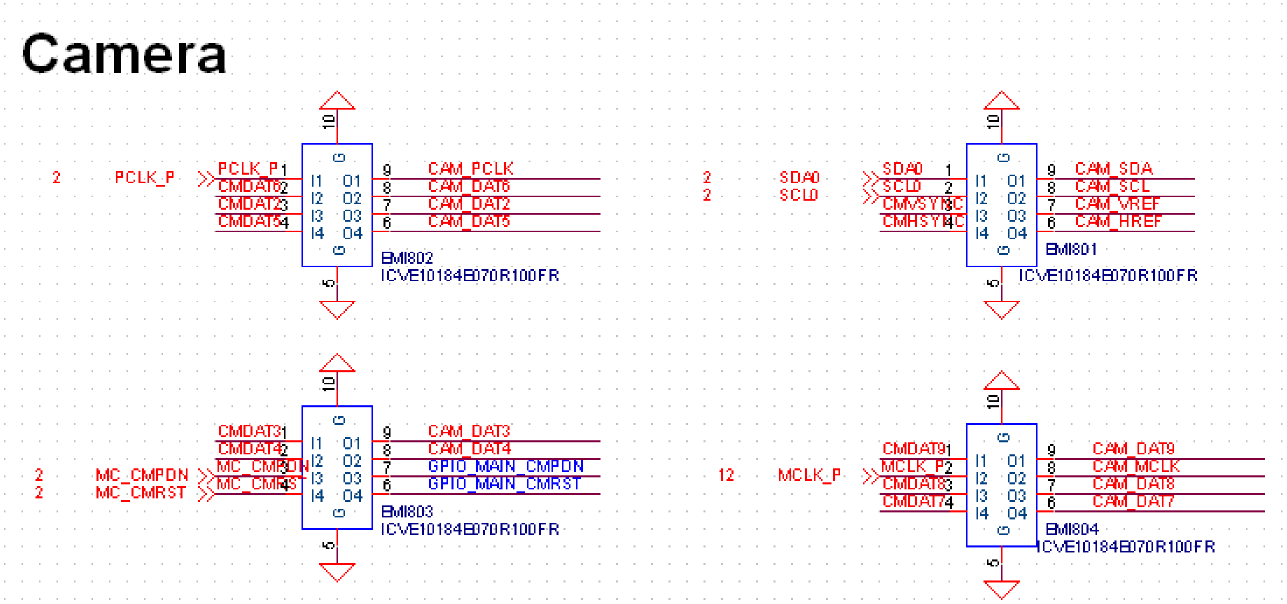
Schematic Notice – Camera (5/x)

- Application circuit of rear facing camera
  - EMI801/EMI802/EMI803/EMI804 are for desense-free proposal.
  - It is recommended to reserve common-mode choke to prevent RF de-sense, the max. cap loading of common-mode choke must be less than 3pF.



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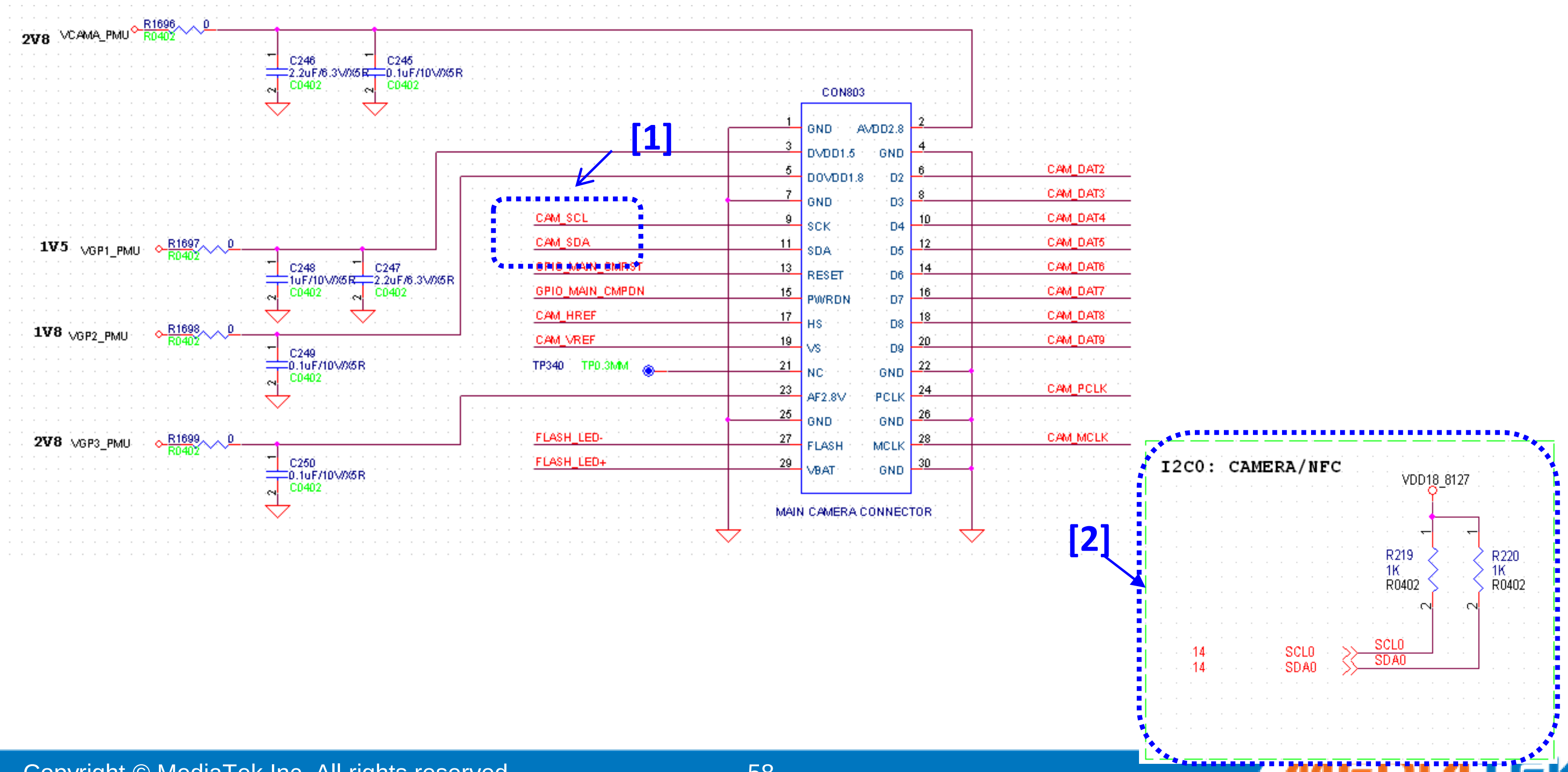
Schematic Notice – Camera (6/x)

- Application circuit of rear facing camera
  - I2C control interface
    - The I2C-0 (SCL0 & SDA0) is used to control the main and sub-camera sensor module. [1]
    - Must have external pull-up resistors for I2C open-drain I/O. [2]



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MT8127 camera capabilities

Application scenario	Rear or front sensor	Interface /throughput	Sensor resolution @ frame rate per sec.
A	Rear (Main)	CSI 4-lane / 1Gbps	8MP@30fps / 13MP@18fps
	Front (Sub)	2 lane CSI / 800Mbps	3MP@30fps / 5MP@24fps.
B	Rear (Main)	CSI 2-lane / 1Gbps	5MP@30fps / 8MP@15fps.
	Front (Sub)	Parallel	2MP@30fps / 5MP@15fps
C	Rear (Main)	Parallel	2MP@30fps / 5MP@15fps
	Front (Sub)	Parallel	2MP@30fps / 5MP@15fps

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MT8127 MIPI DSI/LVDS Design Notice

V0.1

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LCM Design Note – Overview

- Interface
  - Supports MIPI DSI command/video mode, 4-Lane interface
  - Dedicated HW tearing free control pin for MIPI DSI interface
  - The MIPI DSI interface was pin-multiplexed with LVDS interface

- IO Power
  - Support 1.8v IO level LCM (DVDD18_IO3)

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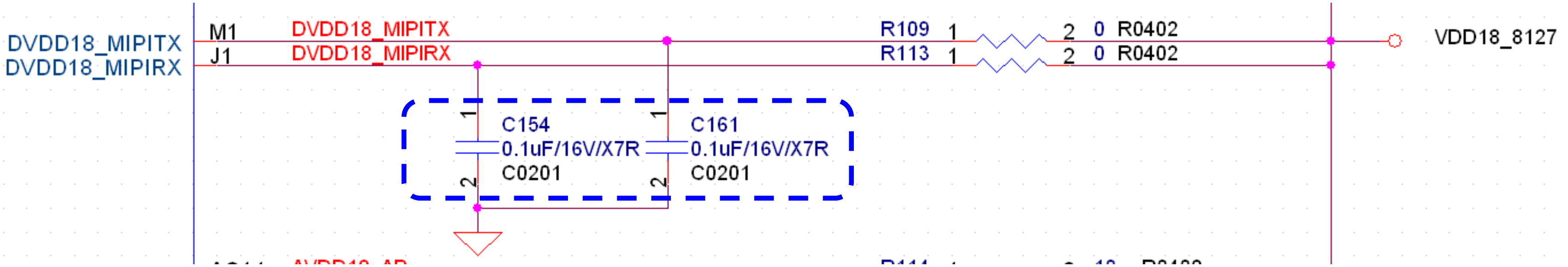
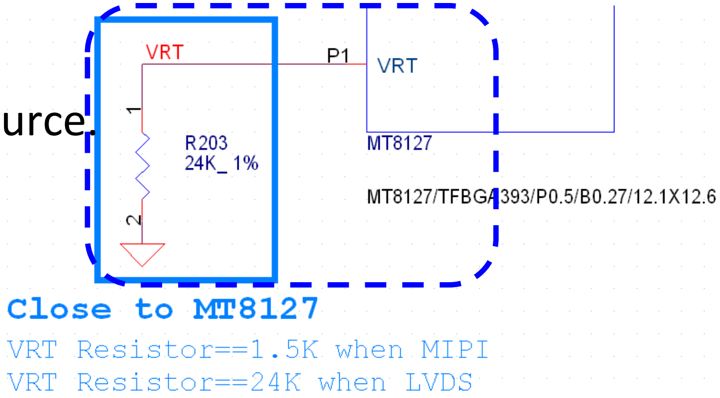
LCM Design Note – MIPI DSI Interface

- All MIPI Power domain connect to 1.8v
- By pass cap for MIPI power domain need to close to BB chip



- MIPI_VRT resistor for MIPI PHY reference current source.
  - When using MIPI Panel VRT==1.5K
  - When using LVDS Panel VRT==24K



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LCM Design Note – MIPI DSI Interface

- BB side design notice
  - MIPI DSI Interface do good to system design simplicity
  - MIPI DSI clk/data are differential pair and trace layout should meet 100ohm differential impedance
    - MIPI_TCP / MIPI_TCN
    - MIPI_TDP0 / MIPI_TDN0
    - MIPI_TDP1 / MIPI TDN1
    - MIPI_TDP2 / MIPI TDN2
    - MIPI_TDP3 / MIPI TDN3

MT8127 MIPI DSI (Pin definition)		LCM side (MIPI Panel)	LCM side (LVDS Panel)
TCP	R4	MIPI_CLKP	LVDS_TDP2
TCN	R5	MIPI_CLKN	LVDS_TDN2
TDP0	P2	MIPI_DATAP0	LVDS_TDP0
TDN0	P3	MIPI_DATAN0	LVDS_TDN0
TDP1	R2	MIPI_DATAP1	LVDS_TDP1
TDN1	R3	MIPI_DATAN1	LVDS_TDN1
TDP2	T1	MIPI_DATAP2	LVDS_CLKP
TDN2	T2	MIPI_DATAN2	LVDS_CLKN
TDP3	U1	MIPI_DATAP3	LVDS_TDP3
TDN3	U2	MIPI_DATAN3	LVDS_TDN3
LCM_RST	W5	/RESET	/RESET

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MT8127 DPI LCM Design Notice

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DPI LCM Design Note (1/x)

- Interface
  - MT8127 Supports DPI 18 bit (RGB666).
  - DPI I/F was pin-multiplexed with other Digital I/O. Mapping table please refer to "**DPI Mapping Table**" as next page.
- IO Power
  - Support 3.3v IO. Please assign 3.3V for DVDD28_DPI.

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DPI LCM Design Note (2/x)

DPI Mapping Table

IO Power Domain	Pin Num	Pin Name	GPIO No.	DPI Netname
DVDD28_DPI	L19	EINT13	**GPIO45**	O:DPI_D0
DVDD28_DPI	M23	PCM_RX	**GPIO20**	O:DPI_D1
DVDD28_DPI	K23	PCM_TX	**GPIO21**	O:DPI_D2
DVDD28_DPI	K24	PCM_SYNC	**GPIO19**	O:DPI_D3
DVDD28_DPI	K22	PCM_CLK	**GPIO18**	O:DPI_D4
DVDD28_DPI	R21	URXD2	**GPIO14**	O:DPI_D5
DVDD28_DPI	P24	EINT7	**GPIO29**	O:DPI_D6
DVDD28_DPI	R22	EINT8	**GPIO30**	O:DPI_D7
DVDD28_DPI	P23	EINT9	**GPIO31**	O:DPI_D8
DVDD28_DPI	U19	EINT10	**GPIO32**	O:DPI_D9
DVDD28_DPI	U20	EINT11	**GPIO43**	O:DPI_D10
DVDD28_DPI	U18	EINT12	**GPIO44**	O:DPI_D11
DVDD28_DPI	R18	EINT1	**GPIO23**	O:DPI_D12
DVDD28_DPI	U22	EINT2	**GPIO24**	O:DPI_D13
DVDD28_DPI	U23	EINT3	**GPIO25**	O:DPI_D14
DVDD28_DPI	V22	EINT4	**GPIO26**	O:DPI_D15
DVDD28_DPI	U21	EINT5	**GPIO27**	O:DPI_D16
DVDD28_DPI	AB19	EINT6	**GPIO28**	O:DPI_D17
DVDD28_DPI	AA21	UTXD2	**GPIO15**	O:DPI_HSYNC
DVDD28_DPI	AA19	URXD3	**GPIO16**	O:DPI_DE
DVDD28_DPI	Y19	UTXD3	**GPIO17**	O:DPI_VSYNC
DVDD28_DPI	V21	EINT0	**GPIO22**	O:DPI_CK

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Thanks

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